C | Imagination

MAGINATION TECHNOLOGIES

GPU'S WITH RISC-Y BASED FIRMWARE PROCESSOR

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World leading technologies in GPU, AI, Wireless Connectivity IP and more

>11 Billion

Cumulative chip shipment with Imagination IPs

\$108M

2018 Revenue

Thousands

Fundamental patents and the only non-US core GPU patents holder

~38%

Mobile GPU IP market share

~43%

Automotive GPU IP market share

#2

In Wireless Connectivity IP

An independent worldwide provider of strategic silicon Intellectual Property

>900 employees worldwide – 80% engineers

An original IP portfolio with a significant, long-present & long-term, patent portfolio underpinning it

Domain expertise in GPU, AI, CPU & Connectivity

Targeting the fastest growing market segments including Mobile, Automotive, AloT, Compute, Gaming, Consumer











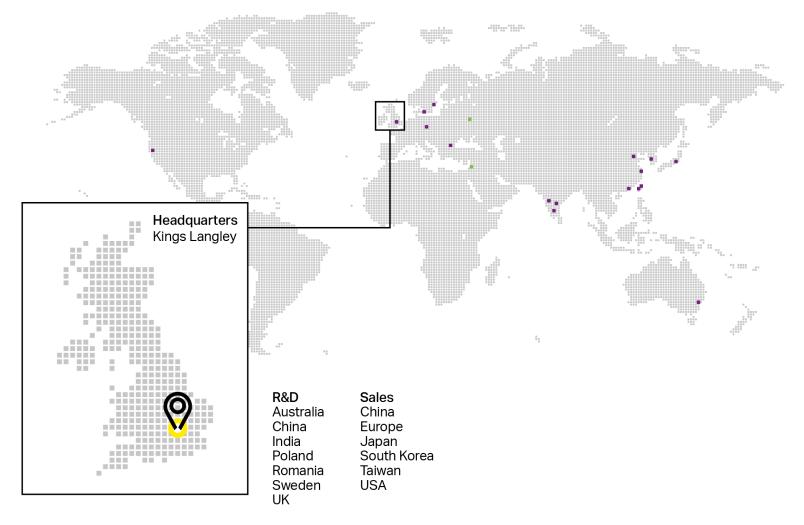






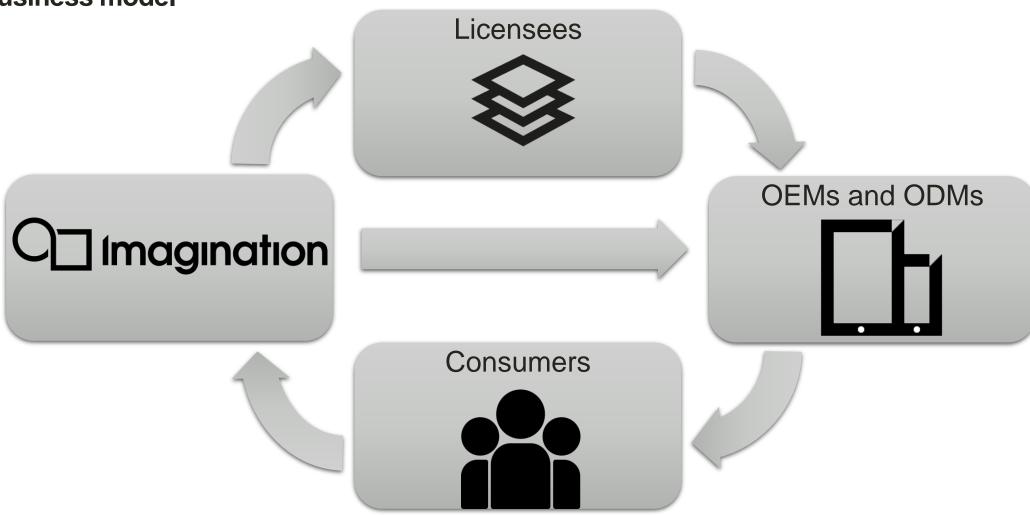


Global Team





Our business model





Imagination

The best solution for embedded graphics, AI, compute and connectivity

Graphics

Broad suite of products covering embedded graphics needs across all markets

Compute

Dedicated Compute & Al hardware IP

Connectivity

Connectivity and broadcast communications

High performance, low power

PowerVR GPU

Scalable cores with best PPA + Safety Critical Automotive Cores

PowerVR Ray Tracing

Architecture for advanced modelling of light

PowerVR NNA

PowerVR Neural Network Accelerators Al Compute Software, Tools & Libraries

EPP

Ethernet Packet Processor

Ensigma RF

Wi-Fi, Bluetooth

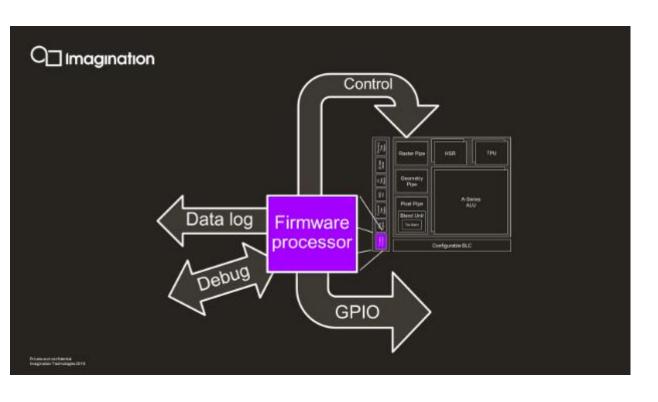
Ensigma IP

Wi-Fi, Bluetooth Digital Radio



Firmware Managed GPU

Maximal Host CPU offloading while maintaining ultimate flexibility



Unique GPU innovation including:

- Concept in use since 1996
- C-Programmable Firmware Code
- Enables:

Local Event Handling

Performance Monitoring

Direct HW Syncs and Control

Direct Power Control via GPIO Signals

Step Debugging of the GPU

GPU Kernel Dump Logs (debug logs)

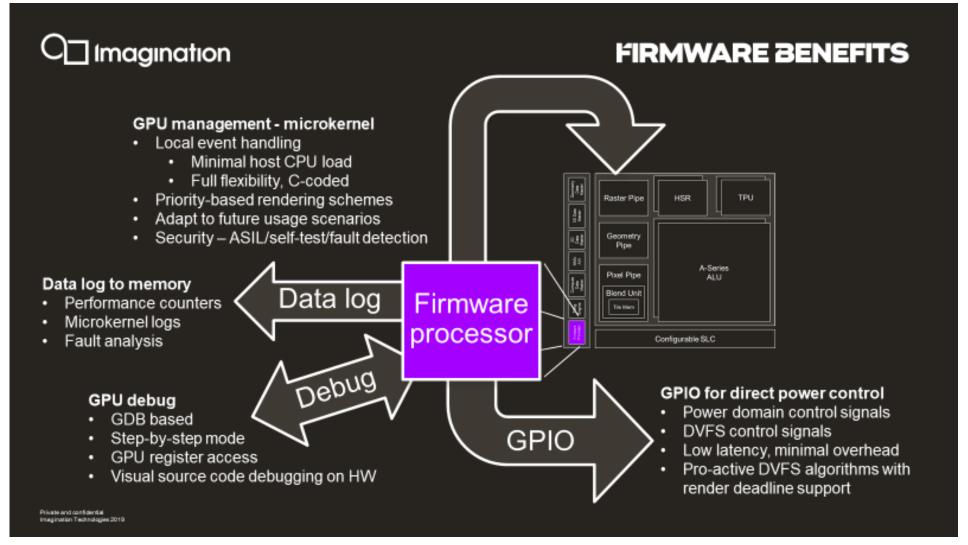
Hardware based virtualisation – multiple clients

Programmable workload priority mechanisms

Now based on RISC-V Architecture



Firmware Managed GPU Benefits

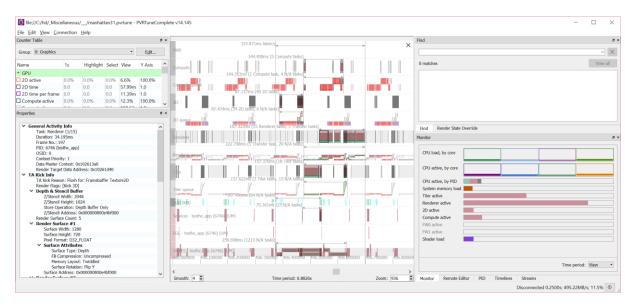




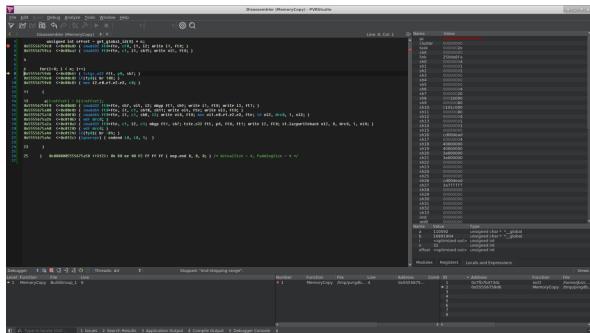
Firmware Managed GPU – Enables Advanced Tool Flows

Enable extensive developer workload optimisation and problem solving

PVRTune – Hardware Performance Profiling



PVRStudio – Hardware assisted GPU Debugger



- Firmware manages performance counters
- Efficient sharing of data with host for analysis

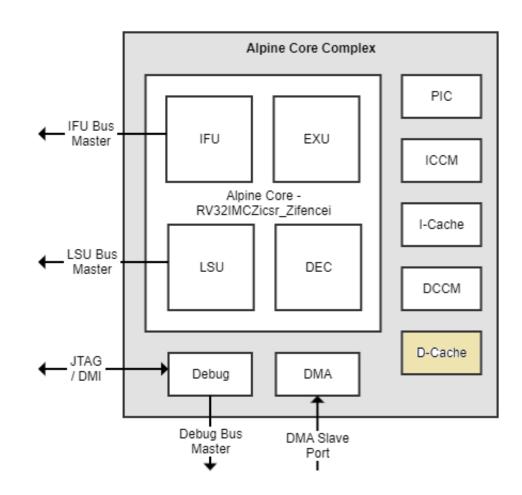
- Firmware runs GDB Server
- Direct Access to HW Registers for debug



Adopting RISC-V as the processor of choice for GPU Firmware Processing

Introducing the RISC-V architecture into the GPU

- Adopting RISC-V to receive benefits from a modern and dynamic CPU architecture
- Alpine core is an adaption from Western Digital's SweRV,
 but with D-cache support
- ECC support to meet functional safety requirements
- Up to 40% faster than previously used processors





RISC-V Tools – Imagination's "Catapult" SDK

We offer a fully-featured RISC-V SDK, including:

- Latest versions of GCC and LLVM compilers, with performance enhancements for SweRV/Alpine
- Optimized picolibc C library
- Catapult Studio IDE, based on VS Code
- Alpine simulator with GDB support
- Available for Linux, Windows and macOS

```
₼ □
 C core_portme.c
C core_portme.h
                                 117 ee s16 matrix test(ee u32 N, MATRES *C, MATDAT *A, MATDAT *B, MATDAT val) {
                                           MATDAT clipval=matrix big(val);
                                          matrix_add_const(N,A,val); /* make sure data changes */
 > simple
 C core list join.c
                                         matrix_mul_const(N,C,A,val);
                                         crc=crc16(matrix sum(N,C,clipval),crc);
                                             void matrix mul_matrix(ee_u32 N, MATRES *C, MATDAT *A, MATDAT *B)

↓ LICENSE.md

M Makefile
                                 #end Basic code is used in many algorithms, mostly with minor changes such as scaling

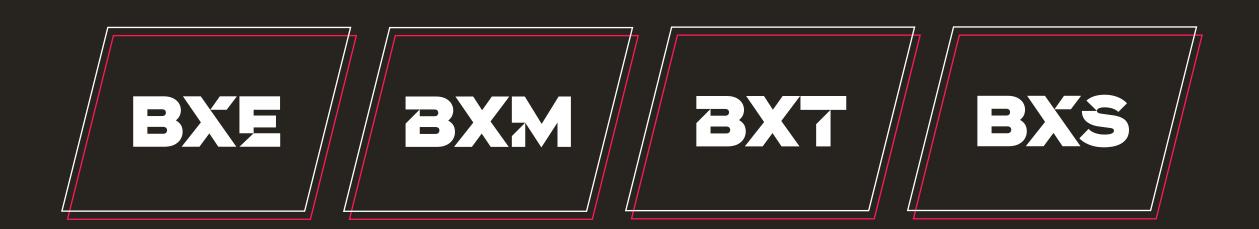
    README.md

                                           matrix mul matrix(N.C.A.B):
M CMakel ists.txt
                                            crc=crc16(matrix_sum(N,C,clipval),crc);
                                 PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL
                                 [proc] Executing command: C:\imgtec\catapult-sdk 0.3.0\build\bin\cmake.EXE --build c:/imgtec/catapult-sdk 0.3.0/examples/apps/c
                                 [build] [6/7 14%:: 0.112] Building C object CMakeFiles/coremark.elf.dir/src/core_util.c.obj
                                 [build] [6/7 28% :: 0.160] Building C object CMakeFiles/coremark.elf.dir/riscv/core portme.c.obj
                                 [build] [6/7 42%:: 0.173] Building C object CMakeFiles/coremark.elf.dir/src/core_main.c.obj
                                  [build] [6/7 57% :: 0.177] Building C object CMakeFiles/coremark.elf.dir/src/core state.c.obj
                                  [build] [6/7 71% :: 0.217] Building C object CMakeFiles/coremark.elf.dir/src/core_matrix.c.obj
                                  [build] [6/7 85% :: 0.232] Building C object CMakeFiles/coremark.elf.dir/src/core_list_join.c.obj
        te: [Debug Semihosting enabled]: Ready 💢 [Catapult SDK clang] 🔞 Build [all] 🛱 🕻
```



IMG B-SERIES

New levels of performance







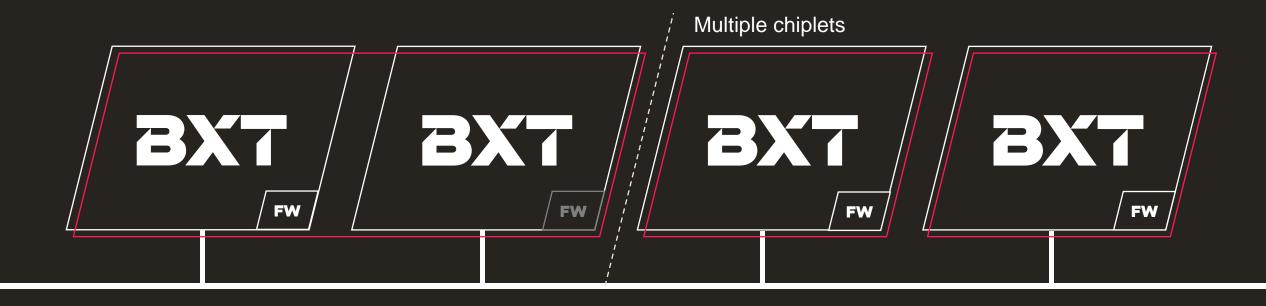
Scaling mobile to the cloud

High-performance
High-efficiency scaling blocks

Decentralised design Greater flexibility Improved layout



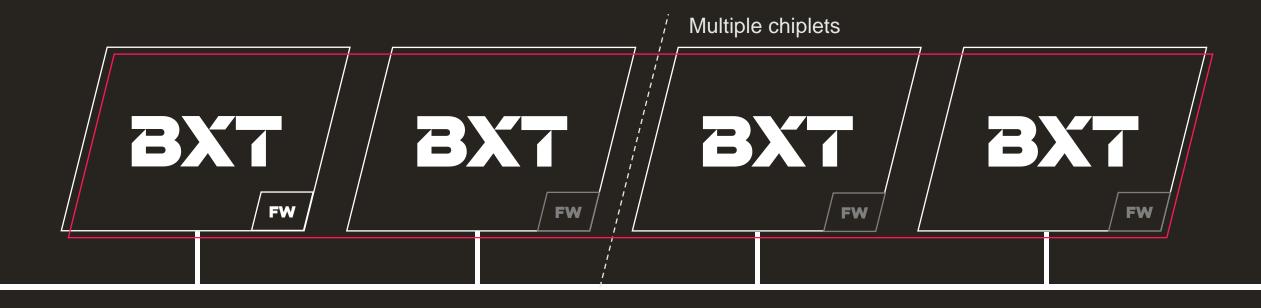
MULTI-CORE



Full flexibility
Multi-primary core scaling



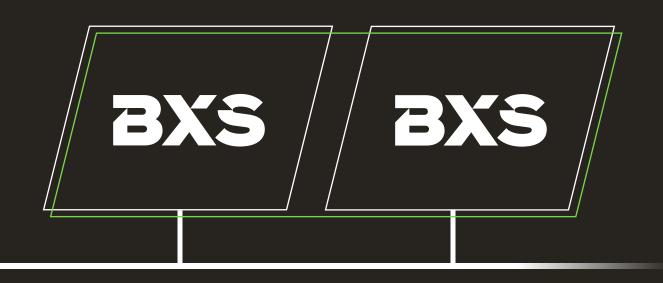
MULTI-CORE



Full flexibility
Multi-primary core scaling



BXS - AUTOMOTIVE



BXS MC2

Automotive-focused performance scaling

Multi-core + TRP highly efficient additional redundancy

Safety delivered without high cost of lockstep

Hardware Virtualisation

BXS AUTONOMY ARCHITECTURE







GPU RANGE

BX7 32-1024 MC1 BXT 32-1024 MC2 BXT
32-1024
MC3

BXT
32-1024
MC4

AXE 1-16M



BXE 2-32

BXE 4-32 MC1 BXM 4-64 MC1 8XE 4-32 MC2 BXM 4-64 MC2 8XE 4-32 MC3

BXM 8-256 BXM 4-64 MC3 BXE 4-32 MC4 BXM 4-64 MC4

BX7 16-512



THANK YOU

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