Imagination

Imagination university programme

RVFPGA

The First Complete Computer Architecture Course Based on RISC-V

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Imagination University Programme November 2020
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The Importance of 「Doing」

4 Key Element For A Winning Lab Package

Hardware

- Low cost: $200
- Fully Featured
- Proven
- Robust
- Debuggable

Software

- Free for academic use
- No limit (code, time)
- Fully debugged
- Online user license
- 「Pocket lab」

Support

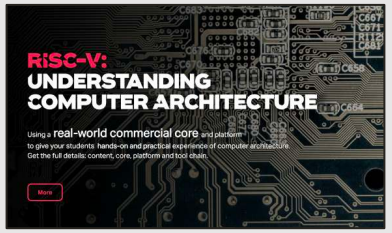
- Responsive active
- Useful information
- Forum / Community
- Email: IUP@imgtec.com
- Knowledgeable

Teaching Materials

- Written by academics for academics
- At least 1 semester
- Complete
  - Slides and lectures
  - Labs and guides
  - Tests and solutions
  - Online videos

  …
- 「Train the teacher」Workshops
- Multi-language and global

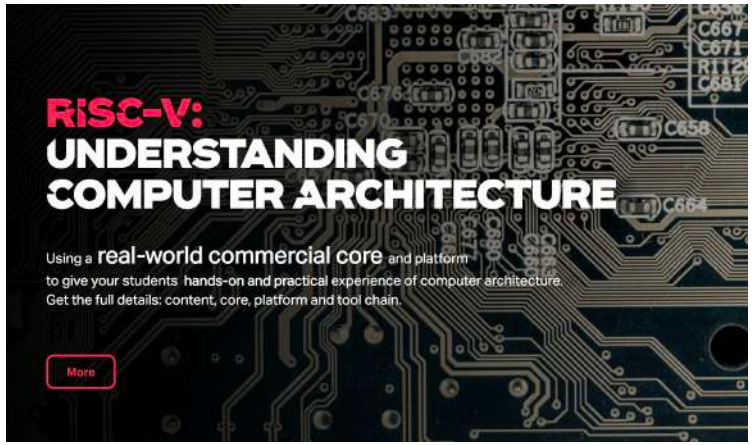
Teaching Projects:

COMPUTER ARCHITECTURE	MOBILE GRAPHICS	EDGE AI
 • 『 RVfpga: Understanding Computer Architecture 』 *(Nov 2020 + Q3 2021)* • 『 Introduction to SoC Design Based on RISC-V 』 *(March 2021)*	 • 『 Introduction to Mobile Graphics 』 v2.0 *Available Now*	 『 Edge AI: Principle and Practice』 *(Mid 2021)*
• MOOC on edX *(2021)* • Textbook: 『 Digital Design and Computer Architecture RISC-V Edition 』 by Harris & Harris *(mid 2021)* • e-Book for developer 『 Guide to RISC-V 』 *(Nov 2020)*	• Hobbyist Self-Study Package: 『 Fun with the BeagleBoneBlack GPU 』 *(Dec 2020)* • Chinese MOOC on Xuetang X *(Nov 2020)*	

RVfpga: Understanding Computer Architecture

Objective:

Influence thousands of future programmers & SoC designers and establish Imagination's reputation in RISC-V.



Teaching Material Basic Infomation	
Authors	Prof. Sarah Harris (UNLV, USA) Prof. Daniel Chaver-Martinez (UCM, Spain) Zubair Kakakhel & their teams
Guidance Panel	The Authors, Ivan Kravets, Ted Marena, Ali Abuassal, Guanyang He, Robert C.W. Owen
Languages	English Chinese Spanish and Japanese
Timing	Started Jan'20, launch Nov'20 (v1) & Q3'21 (v2). Workshops Q1'21
Status	Announced. Getting Ready to Launch e/o November
Platforms	HW Dev't Board - Nexys A7 by Digilent SW: PlatformIO, Vivado Core: Western Digital SweRV
Textbook	『*Digital Design & Computer Architecture RISC-V Edition*』 David Harris and Sarah Harris. *(to be published mid-2021)*

RVfpga: Course Detail

Target Audience:

- Undergraduate students in EE, CS, CE

Track Record:

- MIPSfpga project
  - Based on real-world MIPS microAptiv core
  - Launched April 2015
  - Engaged 800 universities world-wide
  - Winner: Elektra Best Education Support, Europe 2015
- Imagination, a RISC-V User
  - We use RISC-V inside GPU and Connectivity IP products
  - More to experience 金 16:00 with Kristof Beets

Textbook:

- 『Digital Design & Computer Architecture RISC-V Edition』

The Harris & Harris book is the most popular on this subject.
(to be published mid-2021)

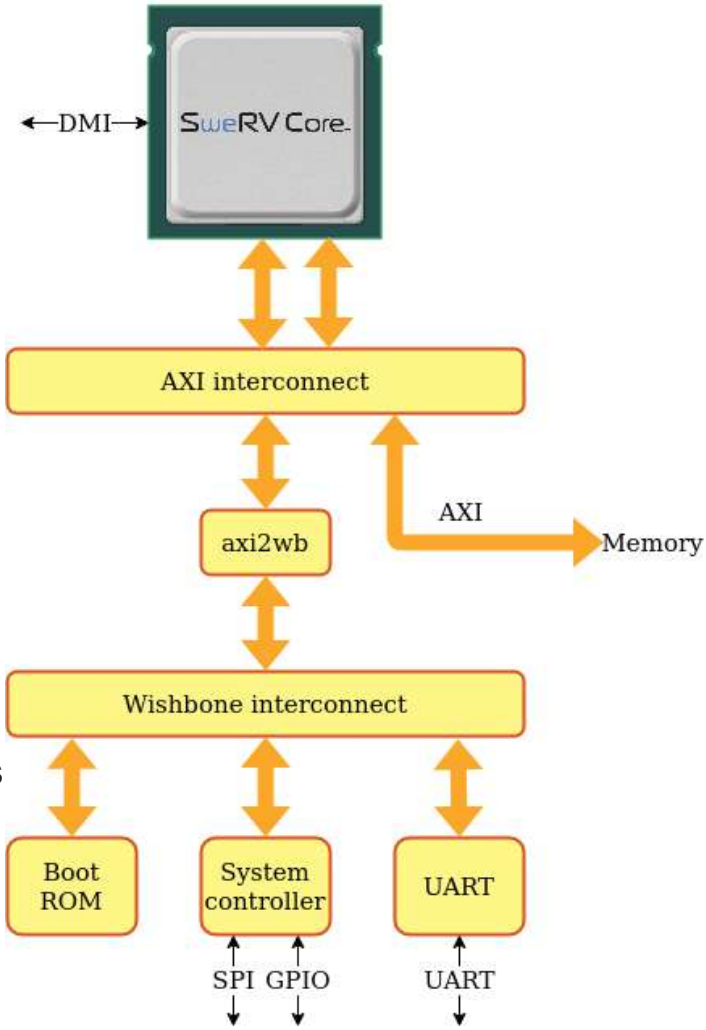
The Core:

- Chips Alliance's SweRVolf SoC

Based on Western Digital's SweRV EH1 core

Future:

- Extend from 10 to 20 labs
- 『SoC Design』master level course
- Global 「Train the Teacher」workshops
- Online learning: Videos and MOOCs



Teaching Materials Package:

RVfpga provides a set of instructions, tools and labs that show how to…

- Target a commercial RISC-V system to an FPGA
- Add more functionality to the RISC-V system
- Analyze and modify the RISC-V core and memory hierarchy

RVfpga: Understanding Computer Architecture
(Undergraduate level)

1) RVfpga Labs Nov'20

Parts 1 & 2: Programming & I/O:

Target audience: Undergraduates

Predecessor Course: Basic Digital design and Computer Architecture

- Students could expand their **fundamental** understanding of a commercial RISC-V core and SoC (RVfpga).
- Students could modify RVfpga to include additional I/O.

2) RVfpga Labs Q3'21

Parts 3 & 4: RISC-V Core and Memories:

- More **advanced,** for 3rd/4th year undergraduates or master's students.
- Students explore and modify the RISC-V core and memory system.

- *The RVfpga Undergraduate Package includes material for a 1 or 2 semester course.*
- *Your course can be built around all or a subset of materials in RVfpga Labs.*

RVfpga: Introduction to SoC Design
(Master level)

RVfpga 『Introduction to SoC Design』 March'21

Masters level course | High level Starter Tutorial

- RTL focused: build the SoC by adding GPIO, UART, DDR
- Software focused: introduce Zephyr & how to interact with the RVfpga SoC
- Hands-on Labs:

  - Lab 1 (RTL): Introduction to RISC-Vfpga SoC.
    Setting up RTL for SweRV, BootROM, GPIO, LED
  - Lab 2 (SW): running bare metal code on RVfpga SoC,
    IDE/Software environment/toolchain setup
  - Lab 3 (RTL): Adding UART and DDR memory controllers
  - Lab 4-5 (SW): Running Zephyr on RVfpga SoC
  - Lab 6 (RTL): Adding SPI to RISC-Vfpga SoC
  - Lab 7 (SW): Using SPI on Zephyr, Accessing Accelerometer
  - Lab 8-9 (SW): Demonstrate Tensorflow Lite on RVfpga SoC

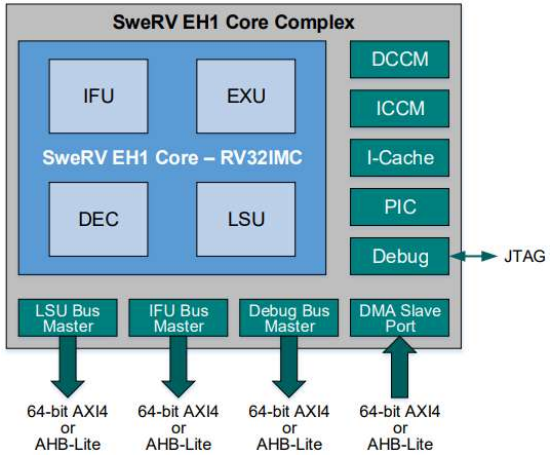
Languages:
English, Chinese (Simplified)
To follow: Japanese, Spanish, Chinese (Traditional)

RVfpga: Key Elements & Costs

Software (free downloads from websites)	
Xilinx	**Vivado** 2019.2 WebPACK
Microsoft	**Visual Studio Code**
PlatformIO	**PlatformIO** with Chips Alliance platform. which includes: RISC-V Toolchain, OpenOCD, Verilator HDL Simulator, WD Whisper ISS.

Hardware (Global Distributors, incl. Digi-Key)	
Digilent	**Nexys A7** (Academic Price $199) - Or Nexys 4 DDR FPGA Board

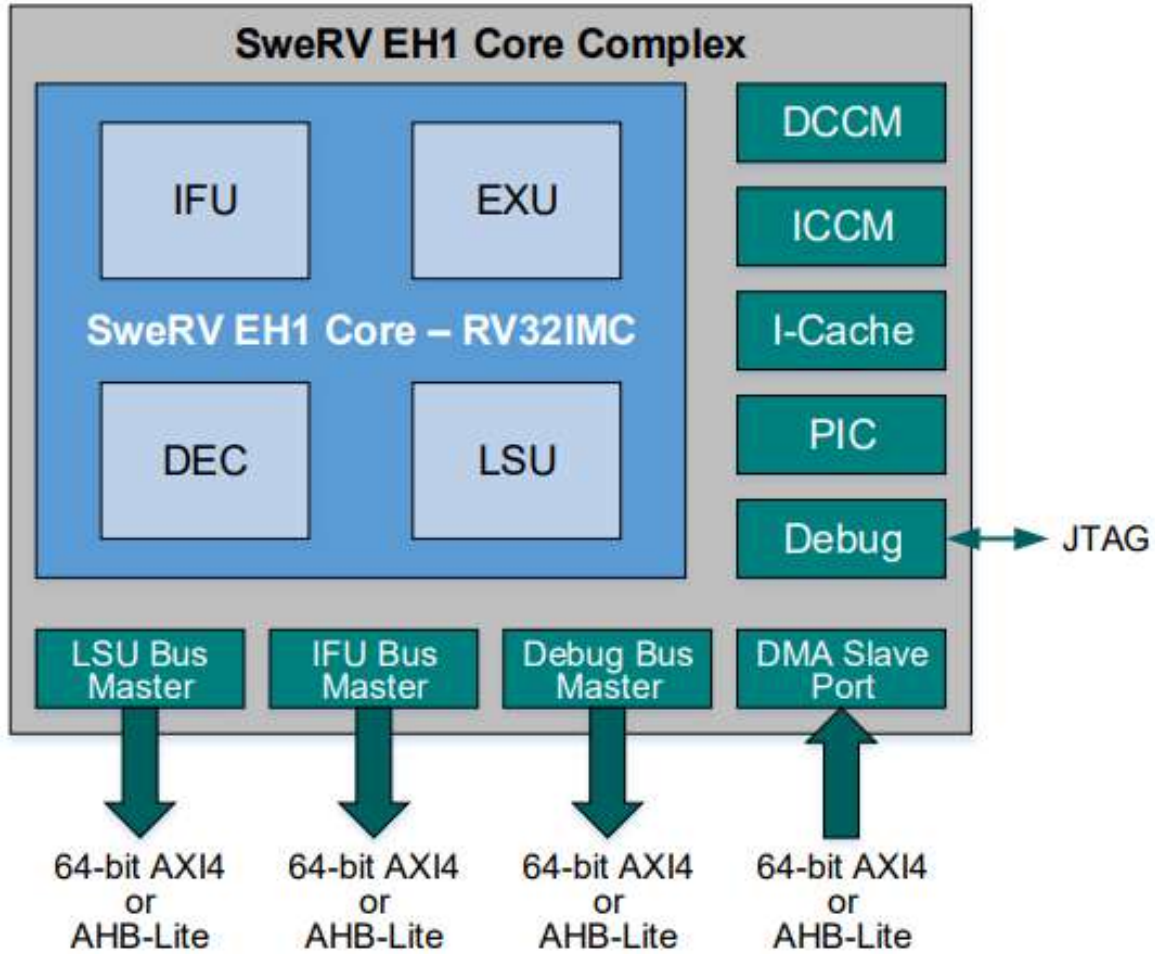
RISC-V Core & SoC (free downloads from websites)	
Western Digital	Core: **SweRV EH1**
Chips Alliance	SoC: **SweRVolf**



RVfpga: SweRV EH1 Core

- RTL of a “real world” core - fully verified, in-production, industrial-grade
- 32-bit (RV32I) superscalar core, with dual-issue 9-stage pipeline
- Instruction sets: RV32ICM
- Separate instruction and data memories (ICCM and DCCM) tightly coupled to the core
- 4-way set-associative I$ with parity or ECC protection
- Programmable Interrupt Controller
- Core Debug Unit compliant with the RISC-V Debug specification
- System Bus: AXI4 or AHB-Lite

No more a “black box” obfuscated or “Education core”…



RVfpga: Sponsors, Contributors & Supporters

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RVfpga Summary: Comprehensive & Complete!

- **RVfpga Getting Started Guide**

  How to install tools, download RVfpga onto the FPGA, load and run programs, and simulate programs running on RVfpga

- **RVfpga Quick Start Guide**

  Abbreviated version of Getting Started Guide

- **RVfpga Labs**

  Part 1: Vivado Project & Programming

  Part 2: I/O Systems

  Part 3: RISC-V Core

  Part 4: RISC-V Memory Systems

- **The RVfpga Package provides:**

  - a **comprehensive introductory RISC-V course**

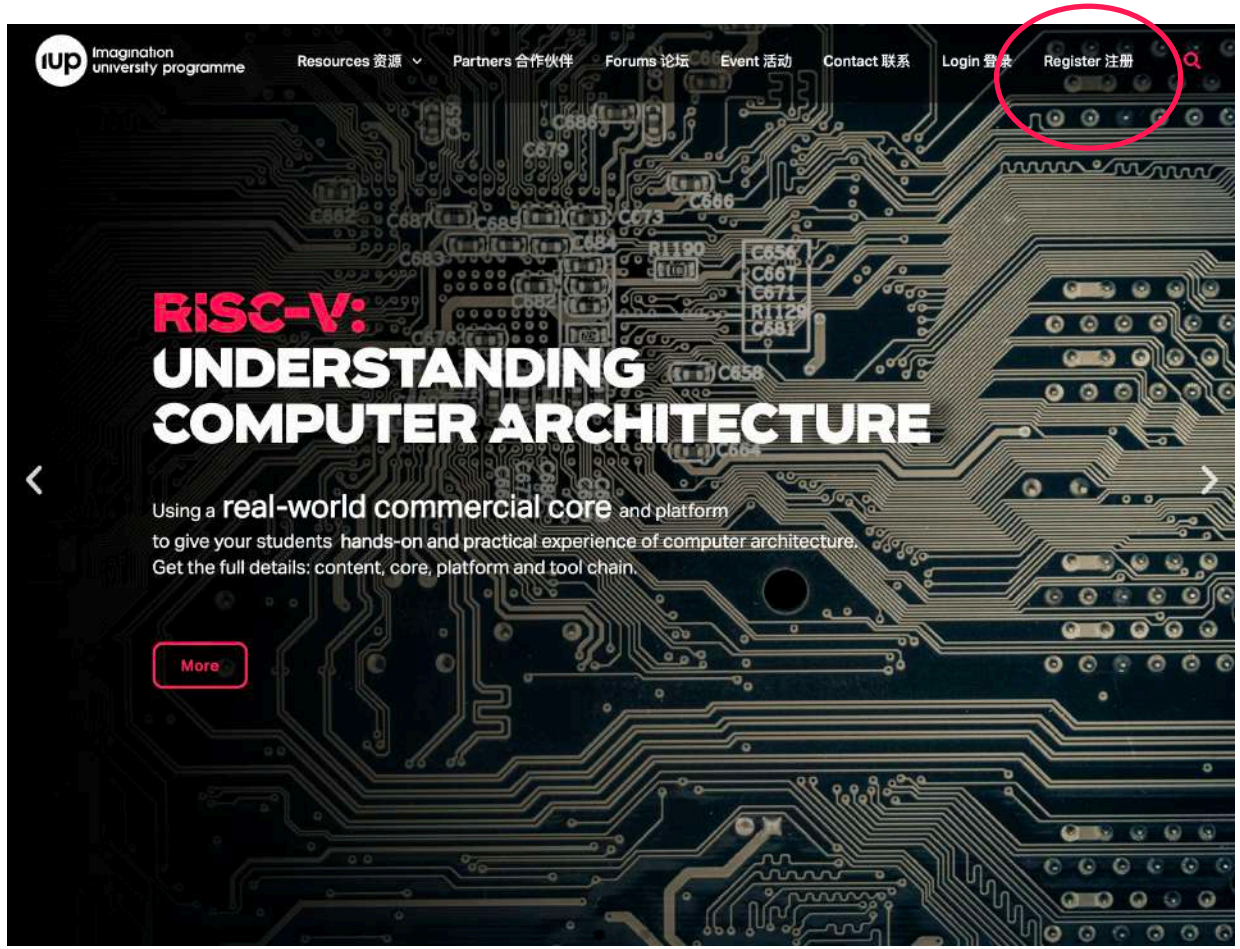
  - a **hands-on** and **easily accessible** way to learn about RISC-V processors and the RISC-V ecosystem

  - a **freely distributed** complete RISC-V course

  - a RISC-V system targeted to **low-cost FPGAs**, which are readily available at many universities and companies.

→ After completing the RVfpga Course, users will walk away with a **working RISC-V processor, SoC and ecosystem**, that they understand and know how to **use and modify**!

The IUP website - our support hub – www.imgtec.com/university



- **Registration**
  Active teachers, researchers and students worldwide
- **Downloads**
  Licensing and delivery mechanism for all our teaching materials, books and software
- **Support Forums**
  - PowerVR Developer Forums
  - RVfpga Forum, AI Forum
  - IUP Forum for curriculum/teaching discussions
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