CloudBEAR

RISC-V processor IP product line

RISC-V 32/64-bit cores product line

CloudBEAR

Small and efficient MCUs

BM series

BM-310
RV32IMCAFNB

BM-610
RV64IMCAFDNB

Fast and compact embedded cores

BR series

BR-351
RV32IMCAFN

BR-651
RV64IMCAFDN

Linux capable application cores

BI series

BI-350
RV32IMCAF

Single issue

BI-651
RV64IMCAFD

Dual issue

BI-671
RV64IMCAFD

Out-of-order

RISC-V 32/64-bit cores product line

CloudBEAR

Small and efficient MCUs

BM series

BM-310
RV32IMCAFNB

BM-610
RV64IMCAFDNB

Fast and compact embedded cores

BR series

BR-351
RV32IMCAFN

BR-651
RV64IMCAFDN

Linux capable application cores

BI series

BI-350
RV32IMCAF

Single issue

BI-651
RV64IMCAFD

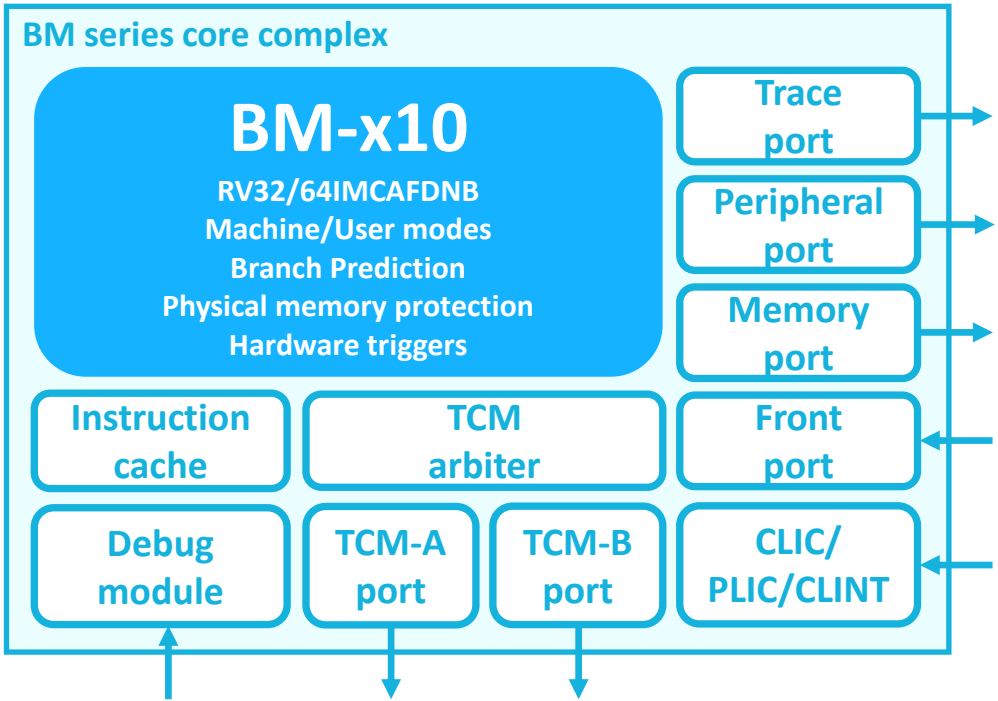
Dual issue

BI-671
RV64IMCAFD

Out-of-order

BM-310/BM-610

- RV32/64IMCAFDNB
- 2-3 stage configurable pipeline, single-issue
- Configurable ports (AXI4, AHB-lite)
- Instruction cache
- TCMs
- Branch prediction (static/dynamic)
- Configurable interrupt controllers
- Debug module
- Trace interface
- Power management



Performance

CloudBEAR

BM-310

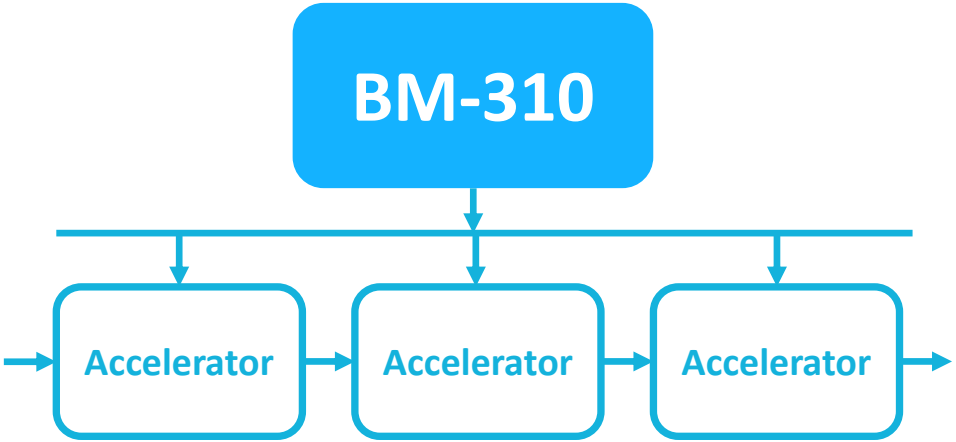
Benchmark (GCC 10.1)	Score/MHz
Dhrystone (ground rule)	1.76
Coremark	3.8
Embench-IoT	1.19*

BM-610

Benchmark (GCC 10.1)	Score/MHz
Dhrystone (ground rule)	1.89
Coremark	3.84
Embench-IoT	1.34*

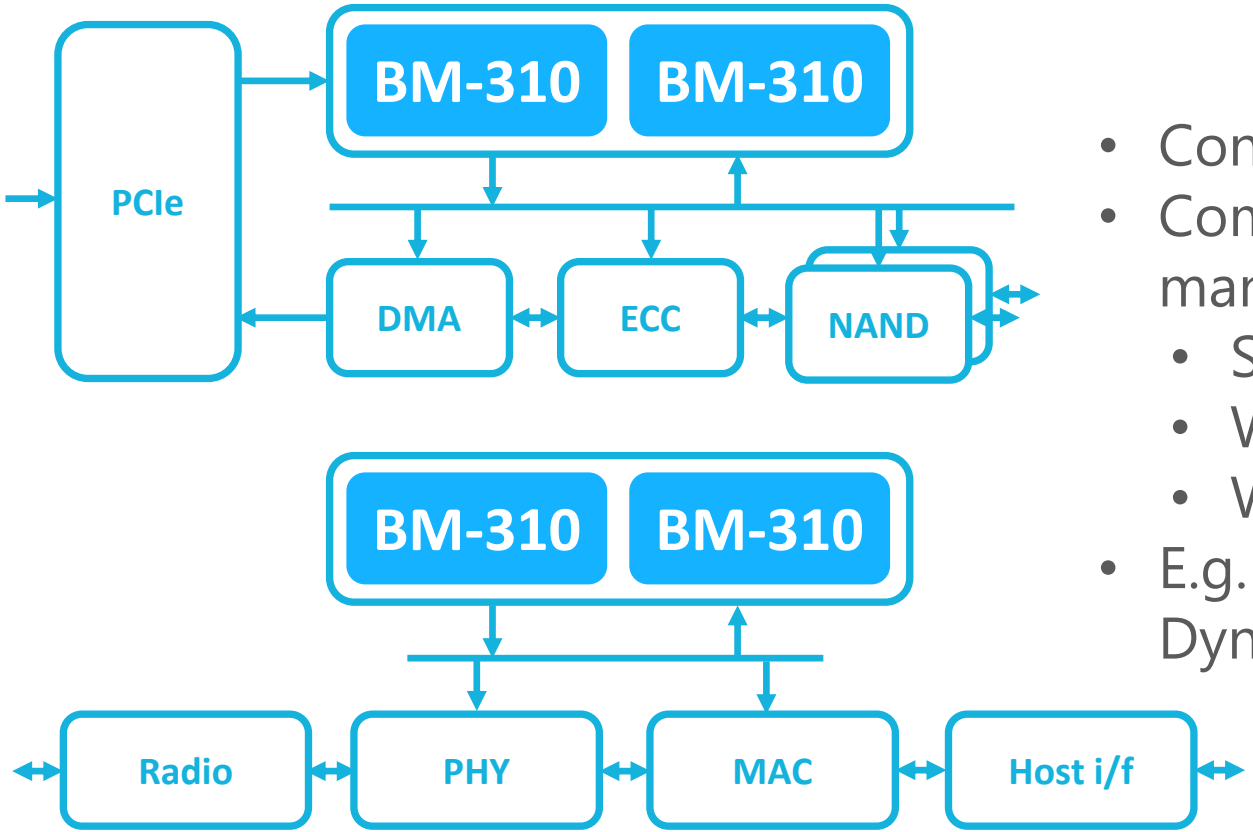
450-700MHz @ 28nm, worst case **
* Performance relative to ARM Cortex-M4 vs RV*IMCB
**Highly depend on process and memory compiler

Deeply embedded applications



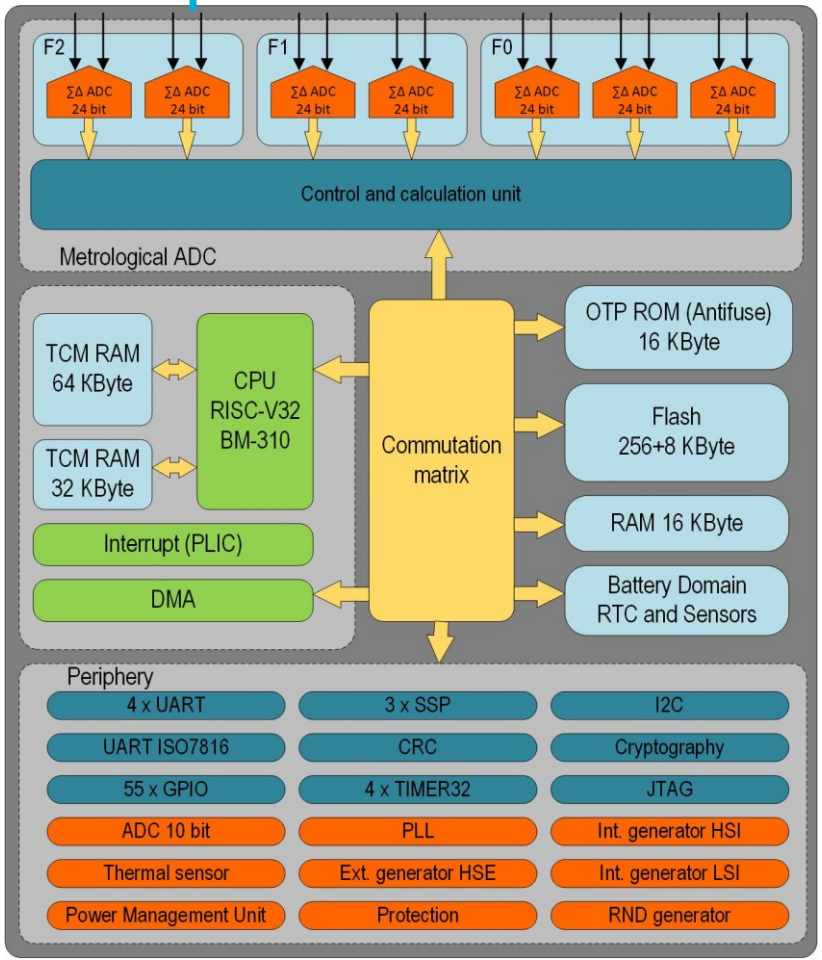
- Control path
  - Networking
  - Wireless baseband pipelines
  - Video pipelines
  - AI accelerators
- E.g. RV32IMC, RV32IC

Deeply embedded applications



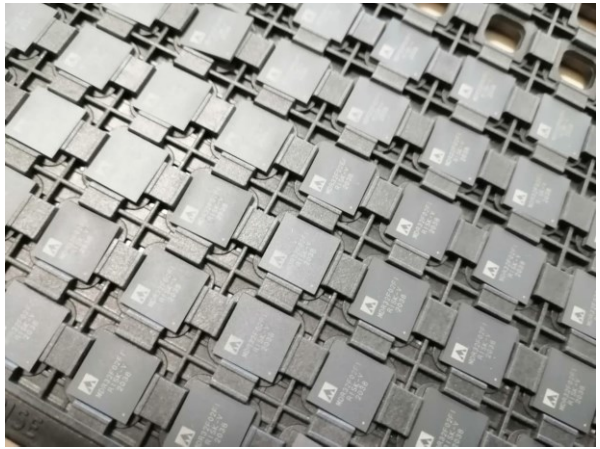
- Control path
- Complex management software
  - SSD controllers
  - Wireless
  - Wearables
- E.g. RV32IMCABN + Dynamic BP

Low power MCU for Smart Metering



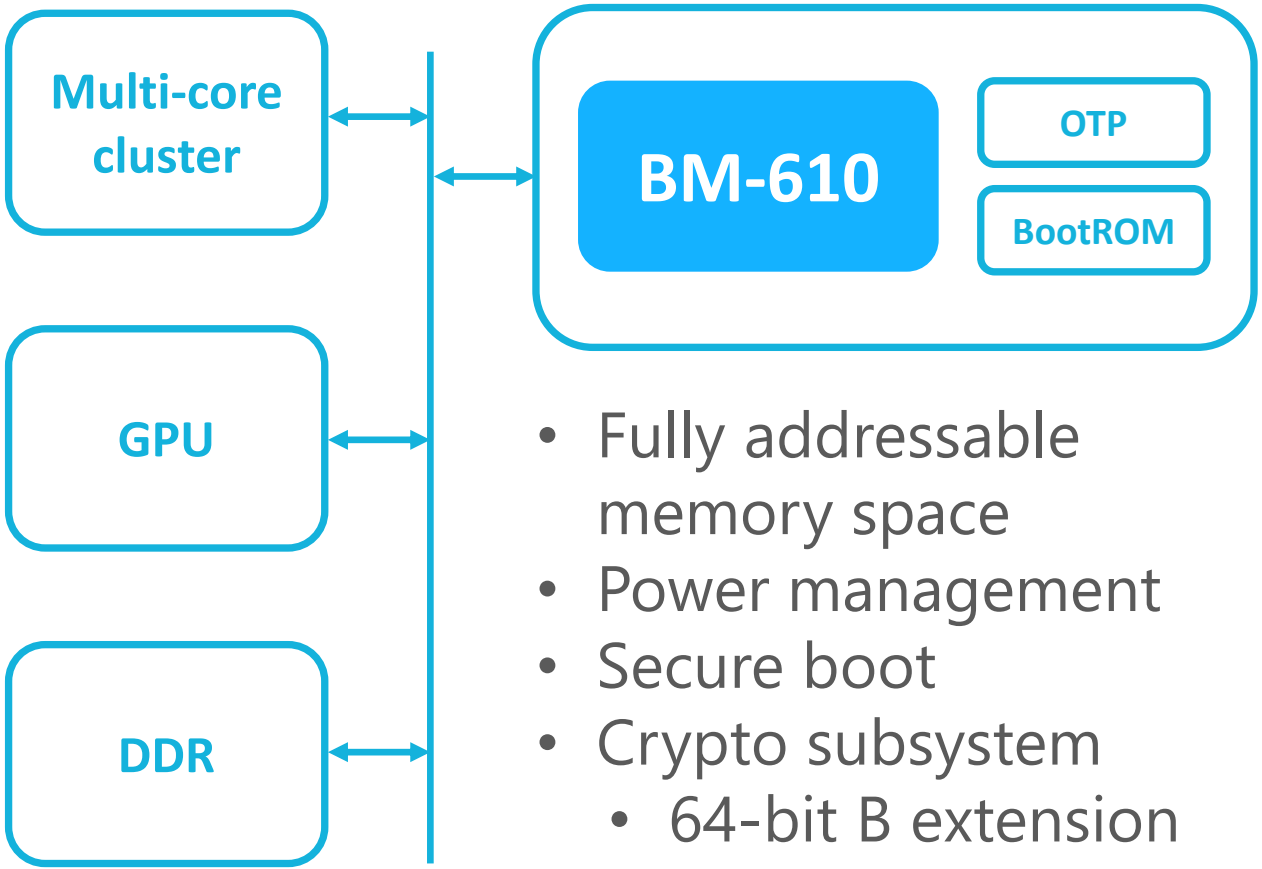
- TSMC 90nm LP
- Customer goes for high volume and low unit price
- Better than Cortex-M4 performance at lower power

Milandr



BM-610 – 64-bit housekeeper core

CloudBEAR



- Fully addressable memory space
- Power management
- Secure boot
- Crypto subsystem
  - 64-bit B extension

RISC-V 32/64-bit cores product line

CloudBEAR

Small and efficient MCUs

BM series

BM-310
RV32IMCAFNB

BM-610
RV64IMCAFDNB

Fast and compact embedded cores

BR series

BR-351
RV32IMCAFN

BR-651
RV64IMCAFDN

Linux capable application cores

BI series

BI-350
RV32IMCAF

Single issue

BI-651
RV64IMCAFD

Dual issue

BI-671
RV64IMCAFD

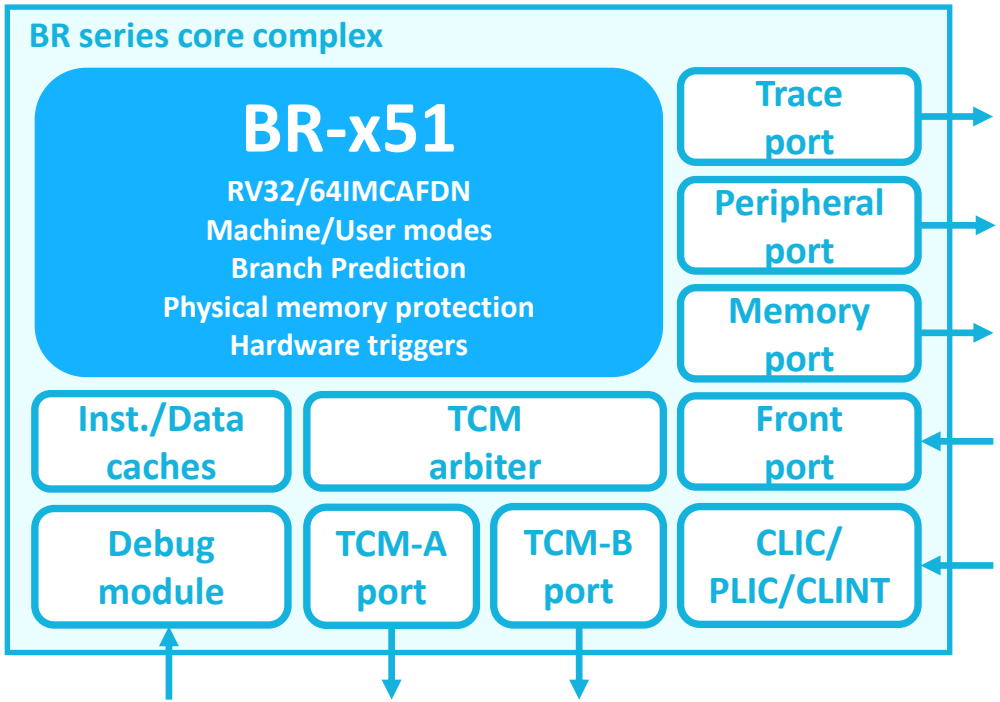
Out-of-order

BR-351/BR-651

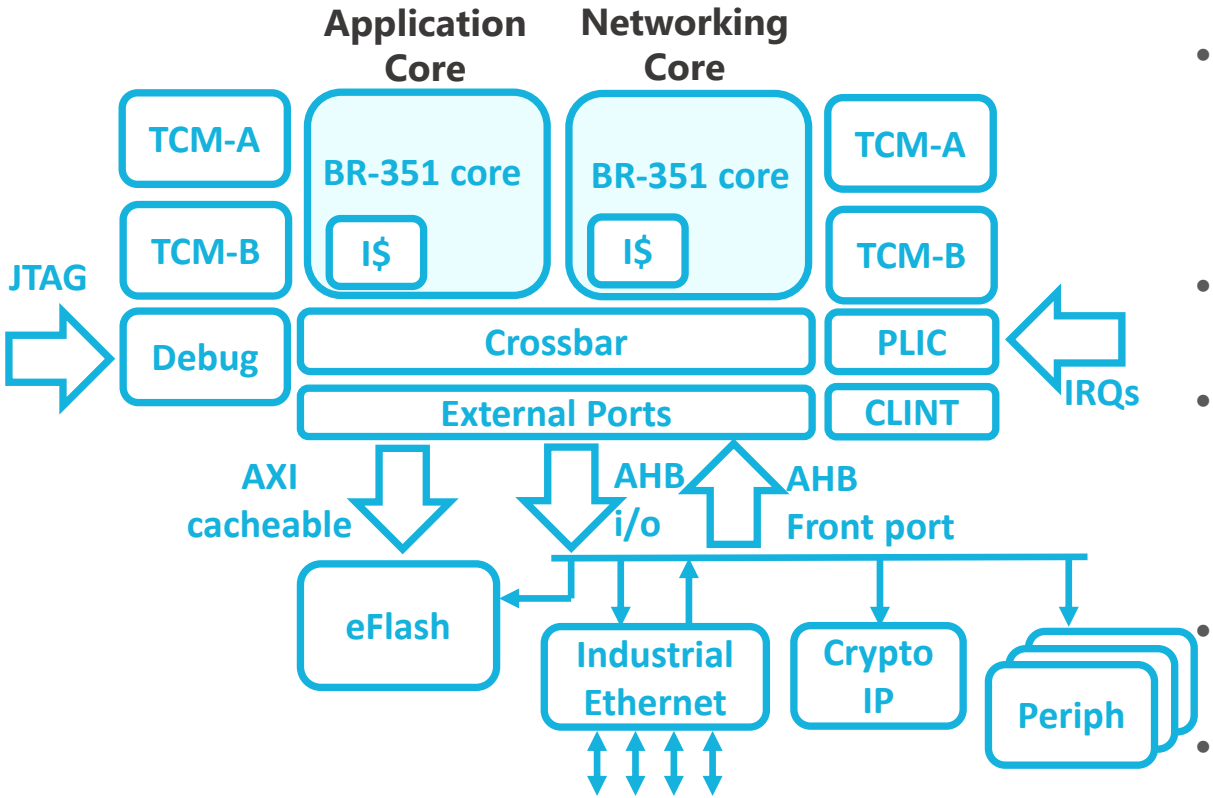
High-performance embedded cores

- RV32/64IMCAFDN
- Dual instruction issue
- 9-stage pipeline
- 1.2GHz @ 28nm worst case

Benchmark	Score/MHz
BR-351 Dhrystone (ground rule)	2.3
BR-651 Dhrystone (ground rule)	2.5
Coremark	5.0

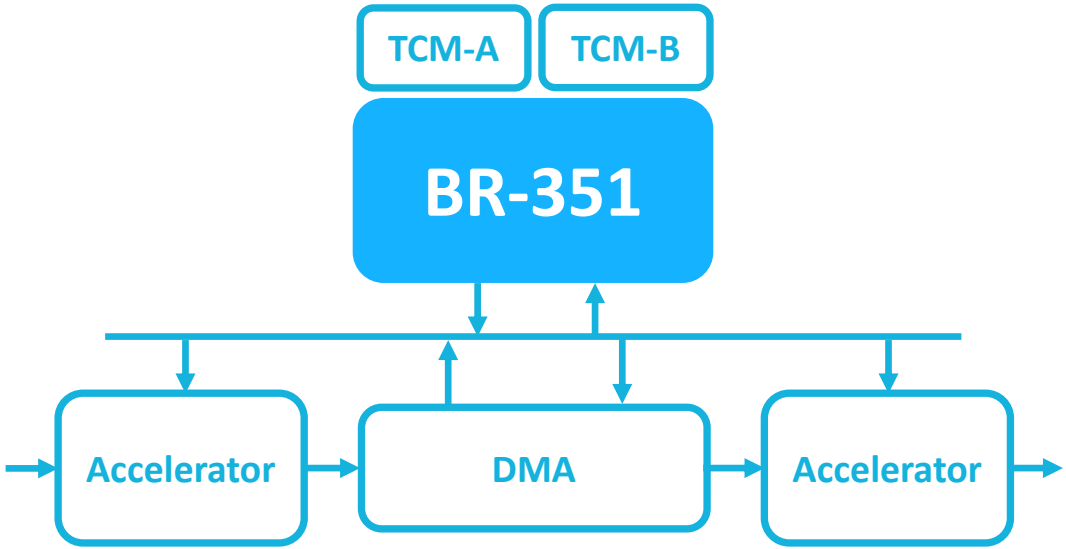


Industrial automation SoC



- Dual core
  - Separate networking core for low latency industrial communication protocols
- PMP for networking/crypto/ application processes isolation
- Low latency
  - N extension
  - Direct access to TCMs from ethernet master
- Execute from the eFlash => I caches with prefetch
- Atomics on buses to support cores sync mechanism

Inline programmable accelerator



- Processing chains
  - E.g. video, networking
- Inline programmable accelerator with 1GHz+
  - Control path
  - Data path

RISC-V 32/64-bit cores product line

CloudBEAR

Small and efficient MCUs

BM series

BM-310
RV32IMCAFNB

BM-610
RV64IMCAFDNB

Fast and compact embedded cores

BR series

BR-351
RV32IMCAFN

BR-651
RV64IMCAFDN

Linux capable application cores

BI series

BI-350
RV32IMCAF

Single issue

BI-651
RV64IMCAFD

Dual issue

BI-671
RV64IMCAFD

Out-of-order

BI series

Linux capable application cores

CloudBEAR

BI-350

RV32IMAC[F]

32-bit Tiny Linux capable core targeting IoT applications

BI-651

RV64GC

64-bit Linux capable core targeting high performance in power constrained environment

BI-671

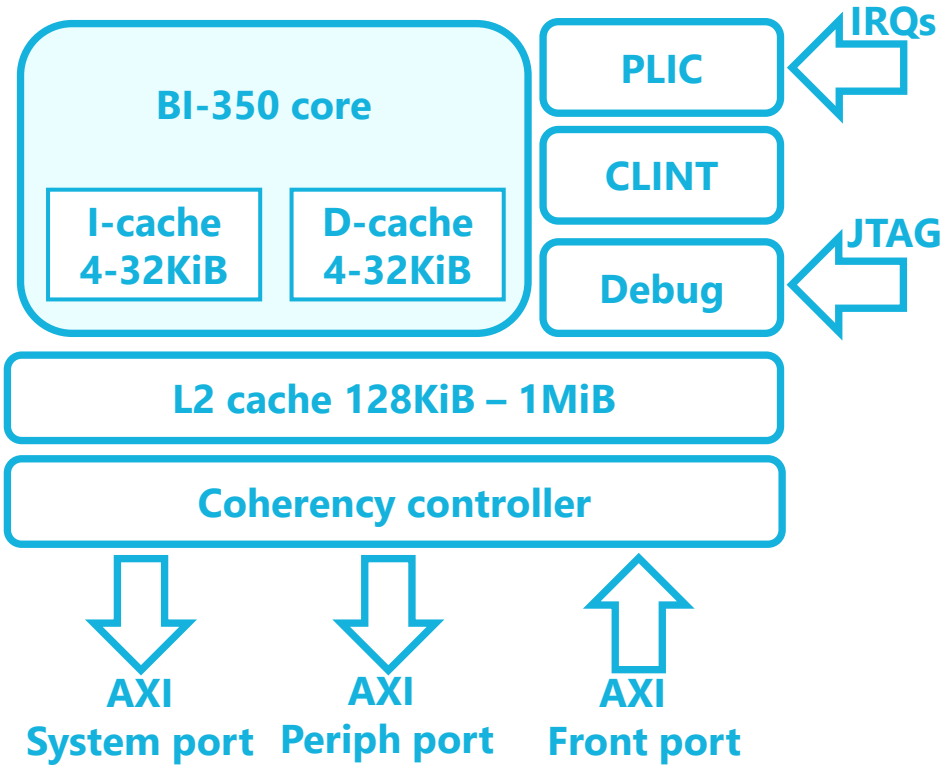
RV64GC

64-bit Mid-range application core for maximum single thread performance

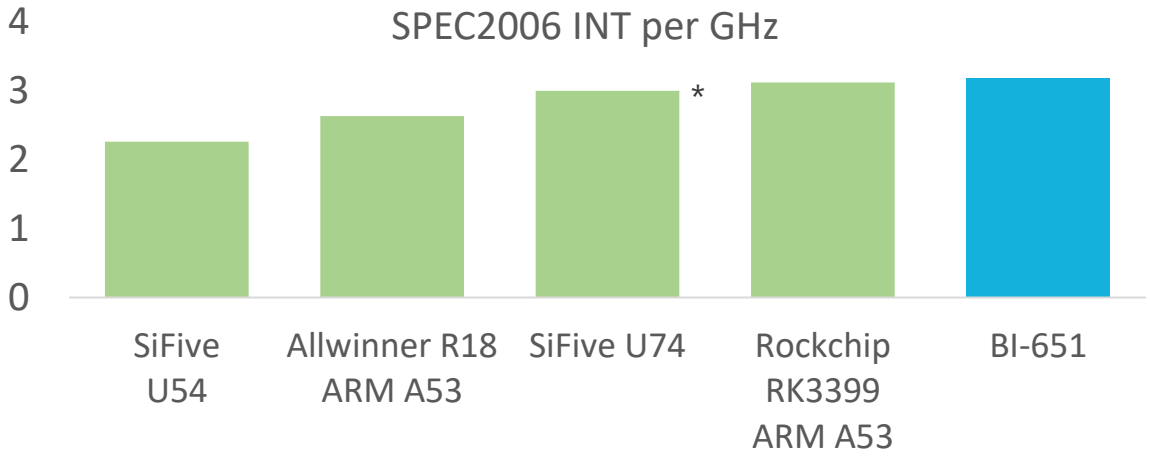
BI-350 small Linux capable core

- Architecture: RV32IMCA[F]
- Single instruction issue
- Machine, Supervisor and User modes
- Configurable caches
  - Smaller size
  - Shorter cache line
  - Narrow memory interfaces
- L2 optional
- Tiny coherency controller configuration
- Configurable BTB, BHT, RAS

Benchmark	Score/MHz
Dhrystone (ground rule)	1.6
Coremark	3.01



BI-651 power efficient dual issue

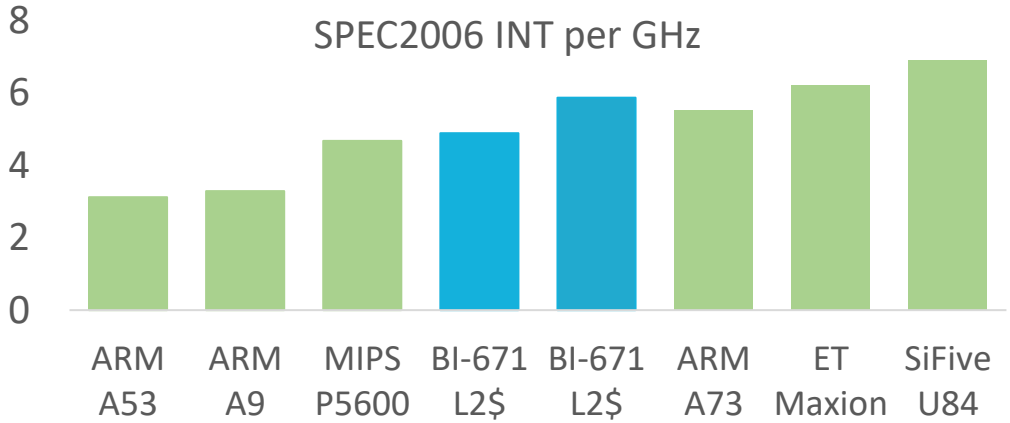


- >1.4x better performance than SiFive U54
- Better than SiFive U74
- On the same performance level or better then ARM A53

Benchmark	Score/MHz
Dhrystone (ground rule)	**2.5**
Coremark	**5.0**

* SPEC2006/MHz score is based on claim that U74 have 2.3x IPC comparing to U84
https://www.sifive.com/blog/incredibly-scalable-high-performance-risc-v-core-ip

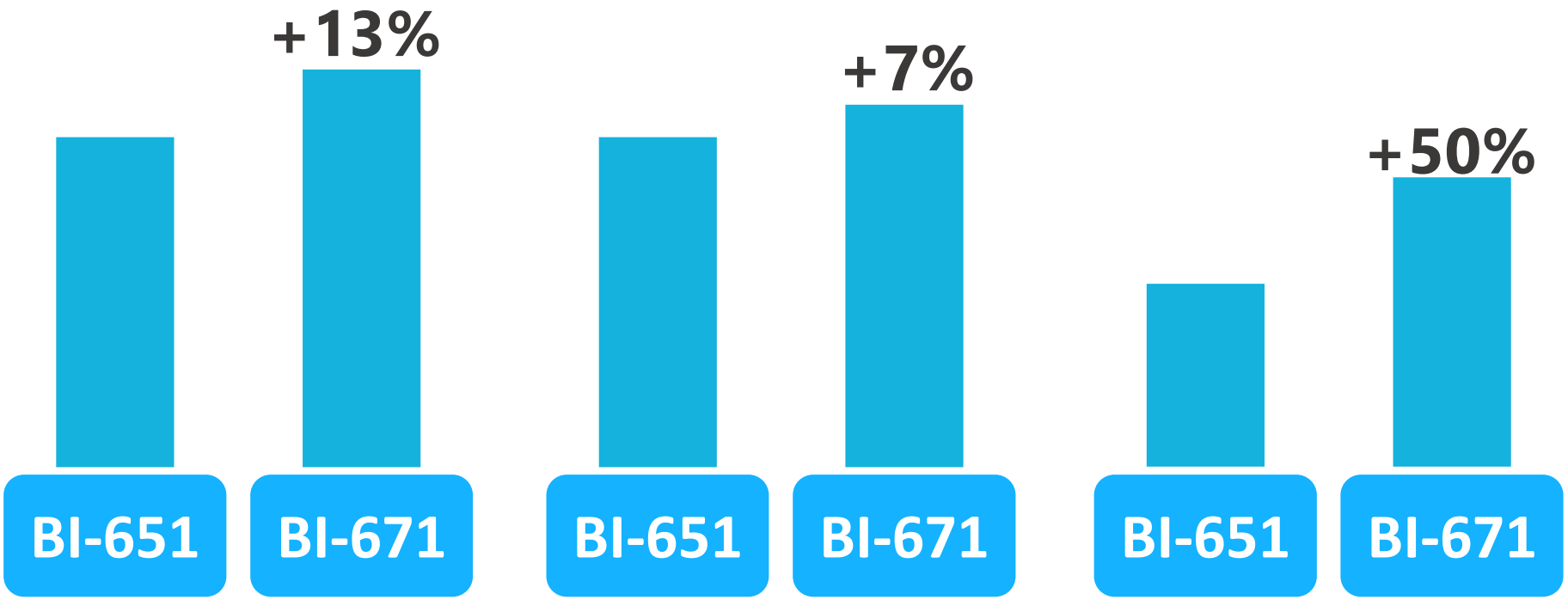
BI-671 performance



- 75-80% of ET Maxion, SiFive U84 performance, but with implementing lesser power and smaller area 2-way superscalar comparing 4-way
- 1.5-1.8x better performance than ARM A53
- On the same performance level with MIPS P5600

Benchmark	Score/MHz
Dhrystone	3.6
Coremark	5.54
	TSMC 28HPC+, 12t
Frequency @ worst SSG	1.2 GHz
Dual core + L2 1 MiB	4.35 mm^2

BI-671 vs BI-651

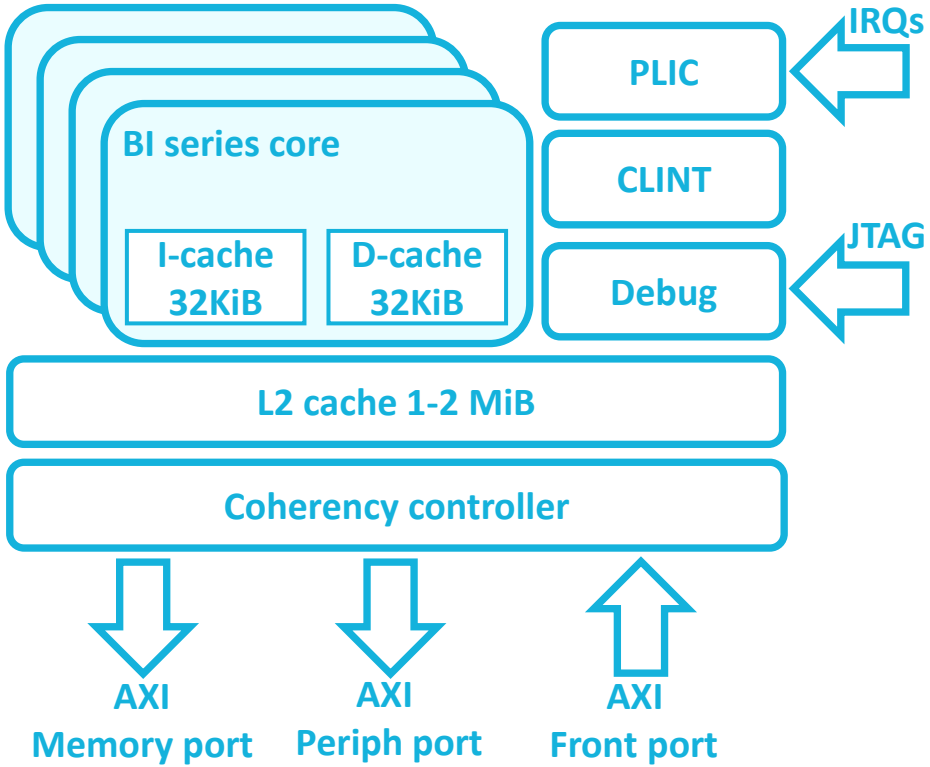


BI series core complex

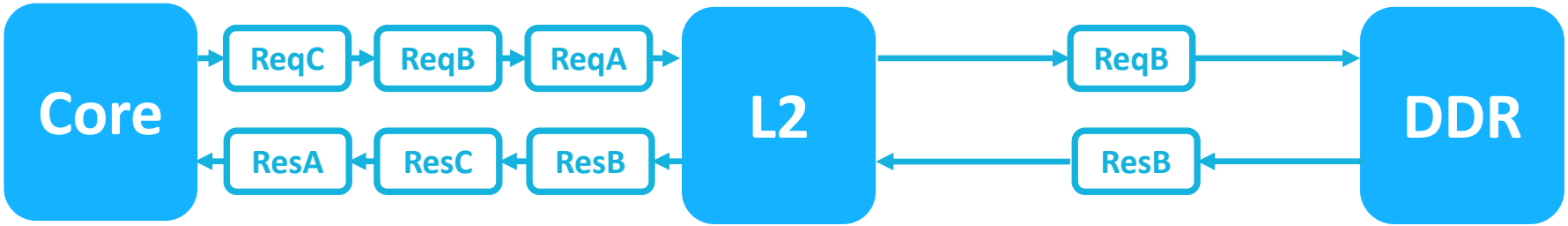
CloudBEAR

Linux capable application cores

- Multi-core fully coherent configuration
- Machine/User/Supervisor modes
- 32 KiB 8-way I/D caches
- L2 cache 1-2 MiB
- Debug module
- Platform Level Interrupt Controller
- Physical memory protection
- Coherency controller for maintaining coherency with peripherals and accelerators



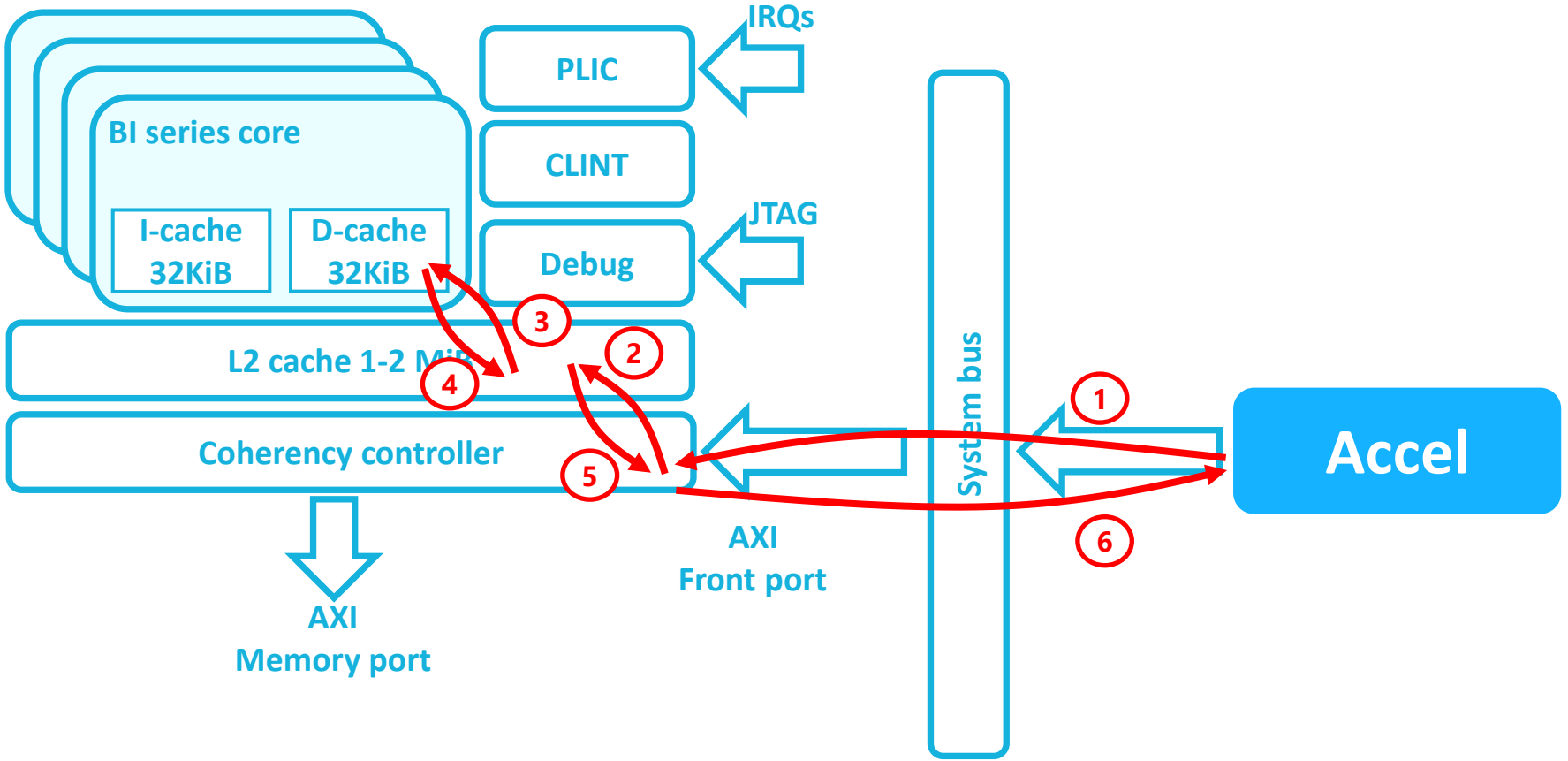
High-performance memory subsystem



- Fully non-blocking caches
  - Cores continue execution of instructions even if cache miss occurs until some next instruction depend on load data
- Multiple outstanding requests in L1 and L2 caches
  - Configurable size of request buffers in L1 and L2

Lightweight coherency control

CloudBEAR



@CloudBEARInc

www.cloudbear.ru