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Ultra Low-Power IoT & AI at the Edge Computing Platform

Optimized For

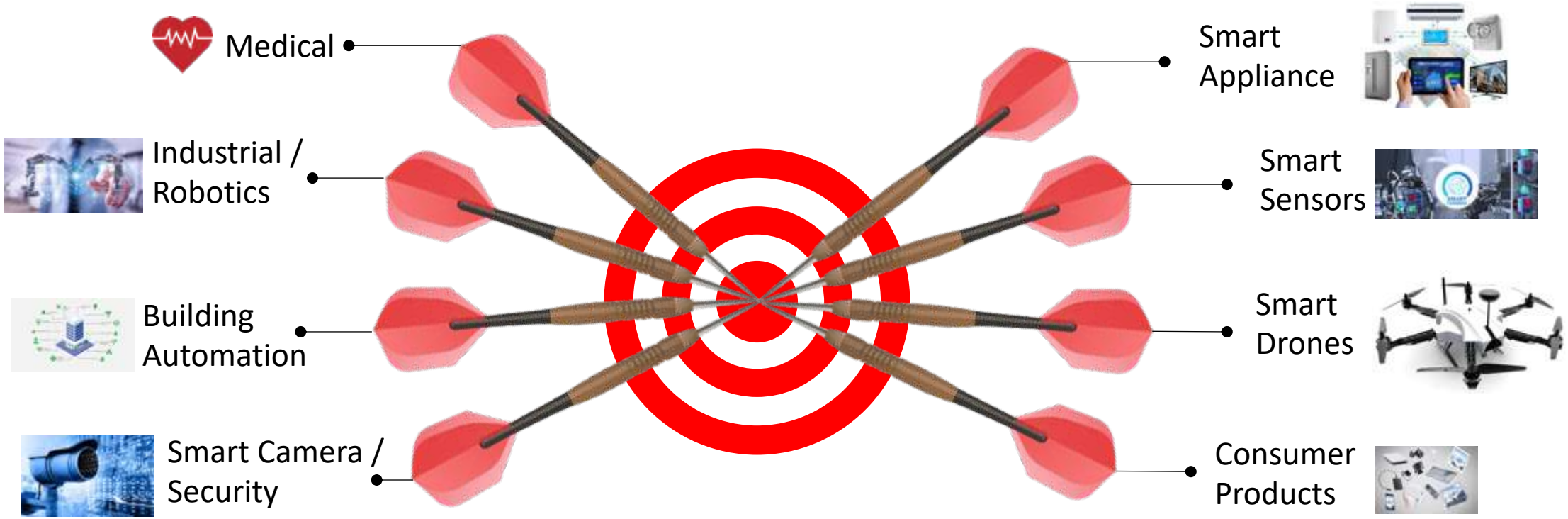
Edge AI/ML, Security, Smart IoT

V3.8

ASA Microsystems Inc.

- Founded early 2018
- Focused on Ultra Low Power High Performance Technology, IP and Products Optimized for *IoT and AI Enabled Edge Computing*
- Based in Silicon Valley with R&D office in Japan
- Multiple Customer Driven Product Developed
- Next generation AI Edge Inferencing products in development
- Experienced Management Team with Proven Track Record

Target Markets



ASA Value Proposition

Ultra low-power high performance RISC-V based processor and ultra low-power vector-based **accelerator** to make **smart IoT** and **edge AI** computing a cost and time to market practical reality.

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ASA RISC-V Processors

Why ASA RISC-V Processors

RISC-V:

- An instruction set – independent of processor architecture and implementation
- Commercial RISC-V processors are proprietary implementations of microarchitecture for the common RISC-V instruction set
- Majority RTL generated from chisel-based implementation of RISC-V processor

ASA RISC-V:

- Proprietary patent pending microarchitecture that implements RISC-V ISA in Verilog
- Ultra-efficient in gate count, die size, and power
- Hyper-scaler clock rate
  - Dynamic range from 100’s of megahertz to gigahertz

ASA RISC-V Based Technology Portfolio

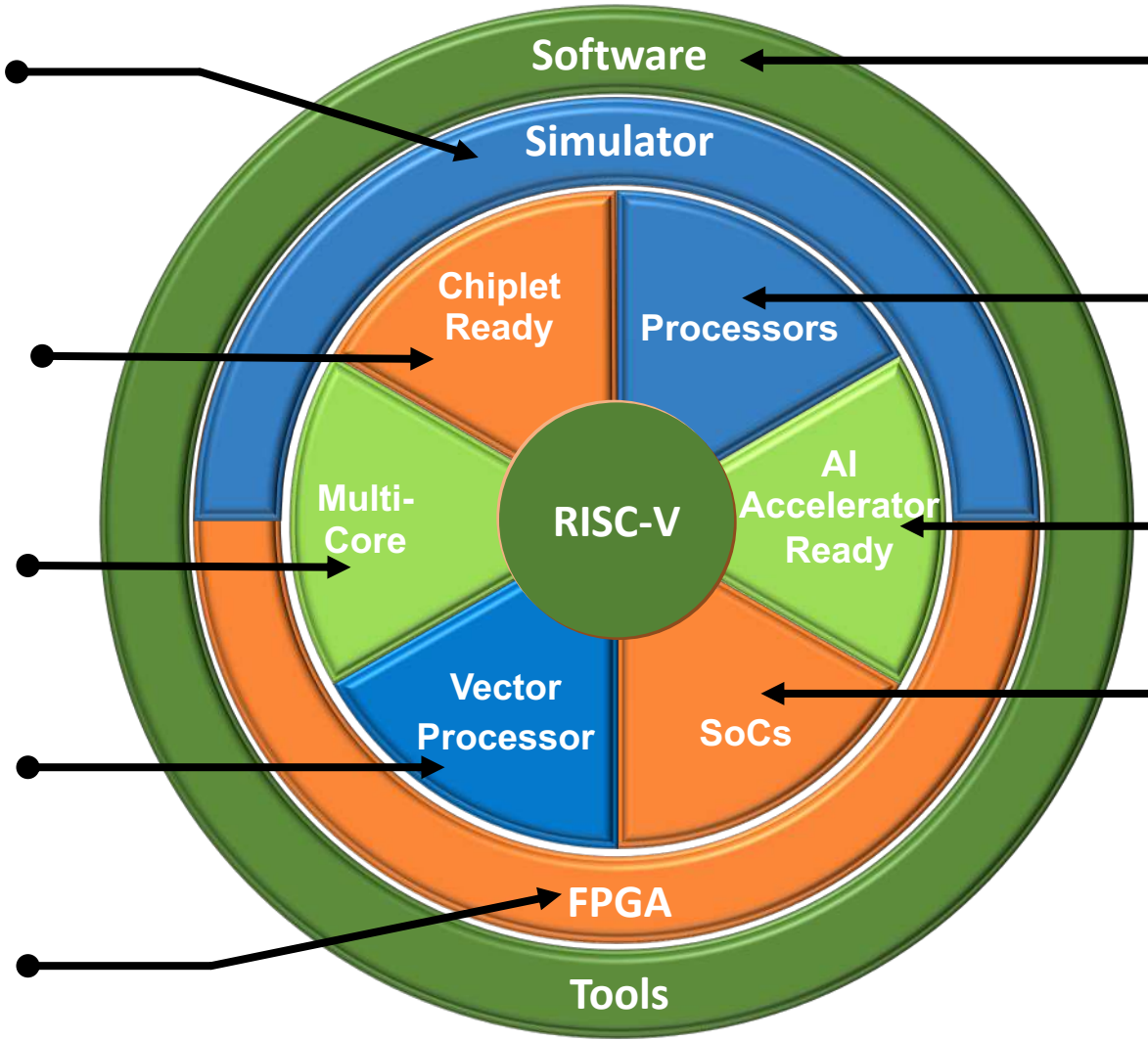
ARSIM: Complete C/C++ based simulator for verification and software development

Heterogeneous chiplet based system design IP and platform

Multicore processor core system platform

Lowest power RISC-V vector processor

Complete FPGA development and production platform



Standard software platform and tools for different applications

Industry's highest performance with lowest power and smallest size RISC-V processors

Tightly coupled custom AI accelerator integration

Fully verified SoC platform for different applications

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ASA Processor Core Family Overview (32-bit RISC-V)

AR32Z

- **Proprietary micro-architecture.**
- Core is ready for customer evaluation.
- **FPGA development platform ready for prototyping**.
- Smallest footprint
- Applications
  - Sensors interface
  - Energy harvesting
  - Battery operated embedded IoT & Medical applications

AR32E

- **Proprietary micro-architecture with parallel execution unit**
- To deliver highest performance at reasonably lower power consumption.
- Small footprint
- Lowest power with highest performance (GHz+ at 28nm)
- Applications
  - Edge computing
  - MPSoC for AI/ML
  - Accelerator coprocessor

AR128V

- **Proprietary micro-architecture with vector execution unit as accelerator**
- High Performance vector operation at lowest power.
- Proprietary Memory Controller
- Applications
  - AI
  - Vision Processing
  - Image Processing/DSP

M0 – M4

M7 and More

128-bit Vector Processor

Optional SIMD/MAC/DSP Co-Processor

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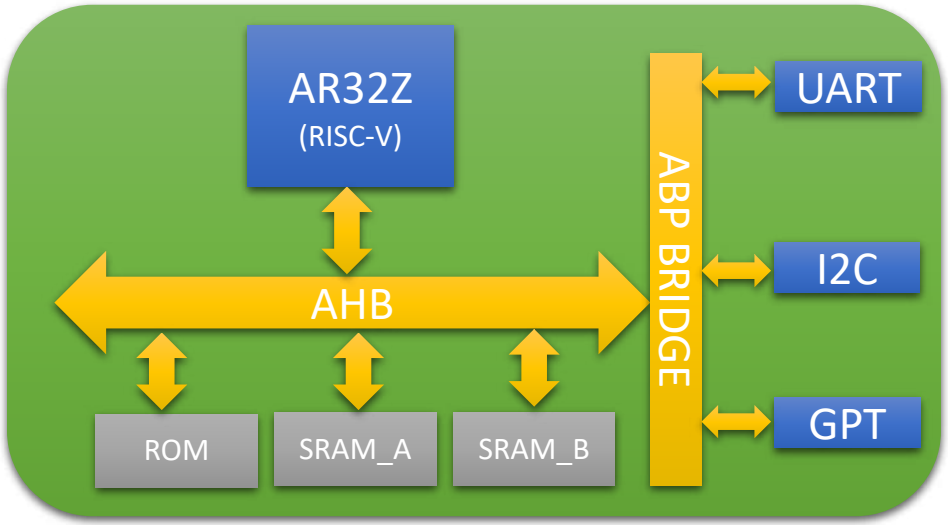
Implementation Results in FPGA

Table shows hierarchical implementation result for the AR32Z SoC (reported core part only) using ARTIX-7-100T device at 100MHz operating frequency

Name	Slice LUTs	Slice Registers	Slice	LUT as Logic	DSP slices	Dynamic Power (mW)
ahb_soc	3,502	2,297	1,245	3,454	4	25
ar32z (ar32z_ahb_top)	1,726	1,005	592	1,678	4	9
core_inst (core)	1,464	639	478	1,416	4	7



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AR32Z vs MicroBlaze in FPGA

FPGA chip : Xilinx Artix-7 100T (speed grade -1)
FPGA Board : Nexys A7
Operating Clock Frequency : 100MHz

	AR32Z	MicroBlaze*
LUT count	1,464	1,550
Dynamic Power	7 mW	31 mW
Total DMIPS	110	90
DMIPS/MHz	1.0	0.9
Board Current Consumption	187 mA	209 mA

* MicroBlaze Processor is generated for equivalent Microcontroller configuration.

MicroBlaze Based Board Power

AR32Z Based Board Power

77% less dynamic power than MicroBlaze

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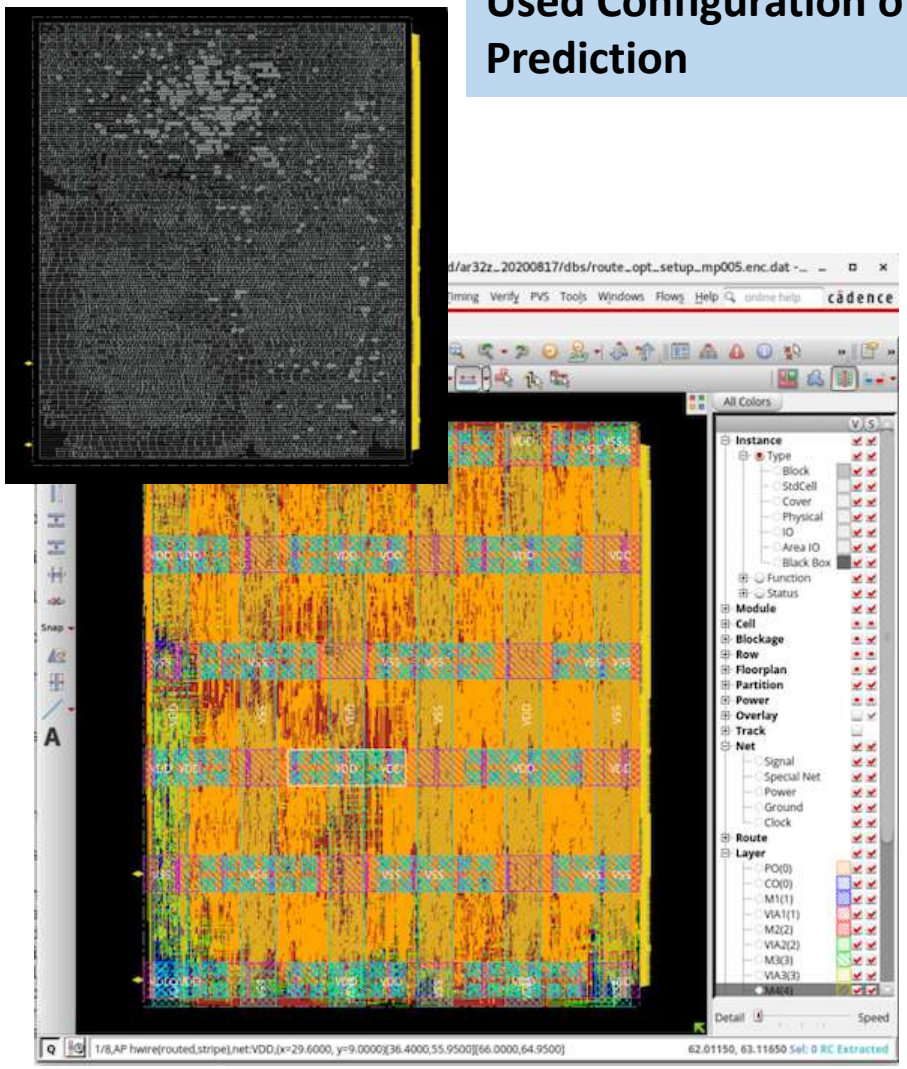
AR32Z ASIC Implementation Results



Used Configuration of AR32Z: RV32IM (Single-Cycle mult.) + Dynamic Branch Prediction

Parameter	Value
Process Node	TSMC 40nm LP
Std Library	Dolphin Tech. 6-track
Clock Frequency	350 MHz
Macro Dimension	121.8 um x 151.9 um
Std. Cells / Flipflops	11,369 / 1,685
Std. Cell utilization	82%

Power Consumption:

Leakage	Total Dynamic Power	Dynamic (uW/MHz)
0.953 mW	2.408 mW	6.879 uW/MHz

Wire Length Statistics (mm):

M1	M2	M3	M4	M5	M6
0.0544	12.08	42.05	44.70	49.39	51.78

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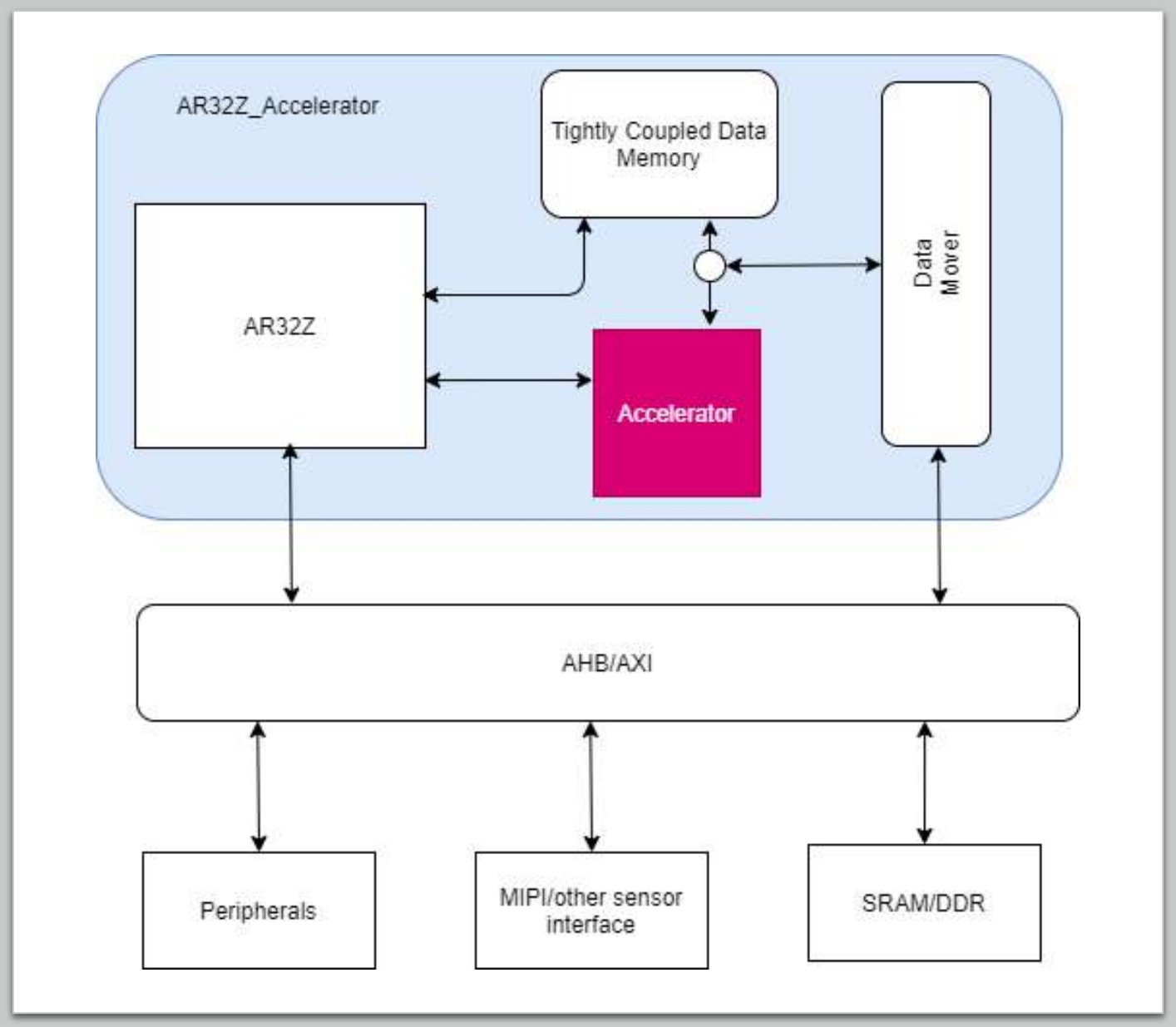
AR32Z feature as AI Accelerator

- Accelerator will be tightly coupled to the processor providing low latency interface.
- Accelerators can come from ASA or 3rd party developers.
- Accelerators can range from DSP to AI inferencing such as image processing, audio processing, DSP and many more.



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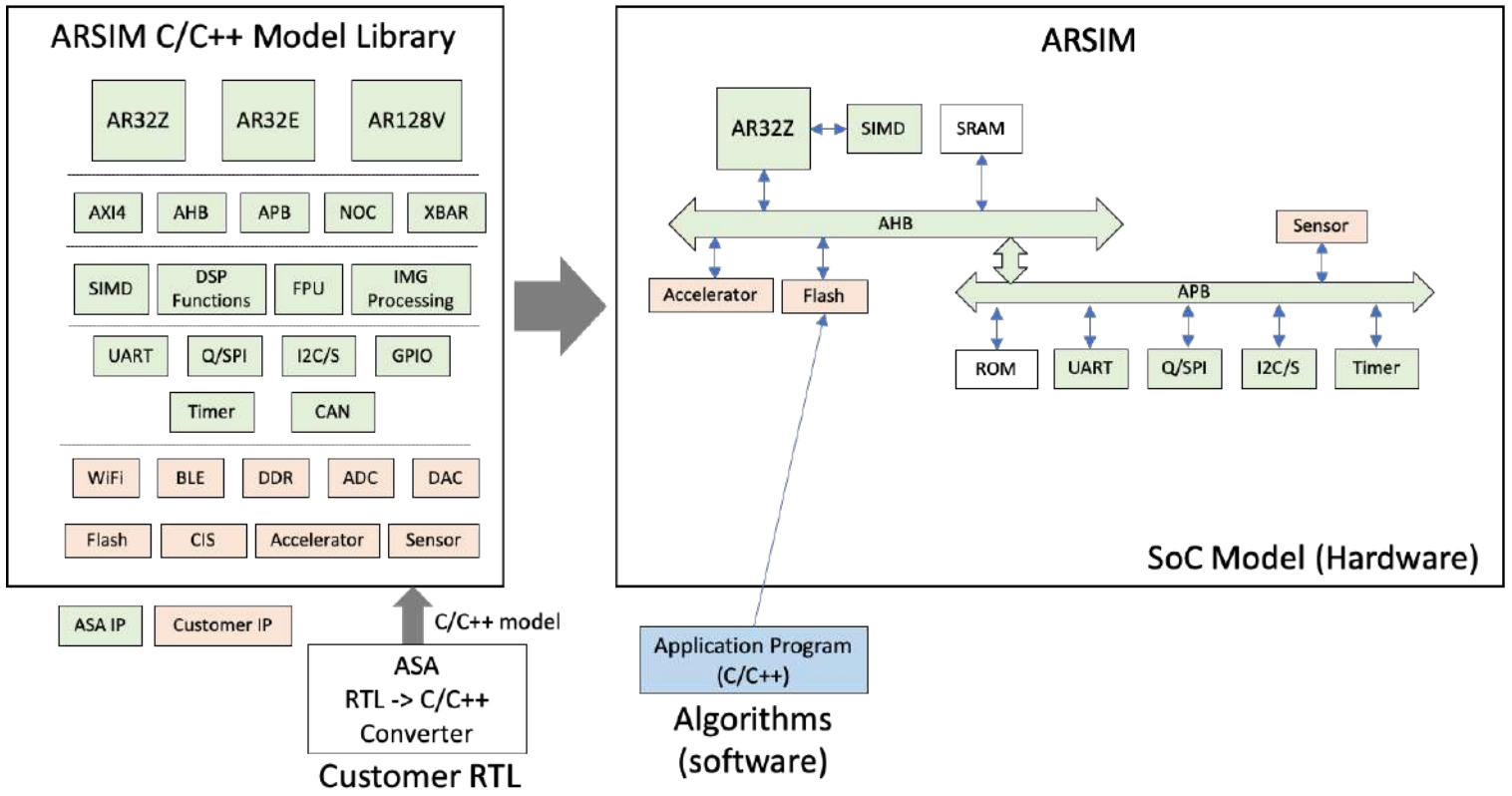
ARSIM (C/C++ Based SoC simulation)



- **C/C++ Model Library:** Most of the required IPs for IoT/Edge SoC is part of this library including ASA RISC-V processor
- **RTL to C/C++ Conversion Engine:** ARSIM conversion engine can be used to convert the customer RTL into ARSIM C/C++ model for ARSIM verification
- **Verification Engine:** customer specific SoC can be dynamically built to create SoC for specific application using the IPs and bus fabrics as part of the ARSIM verification environment. Once the SoC is built, ARSIM enables customers to load the application C/C++ programs into the ARSIM to run the application specific programs to run the verification and analysis of the SoC system
- RISC-V processor from other vendors can also be used

Reduces design verification and design TAT by as much as 30%

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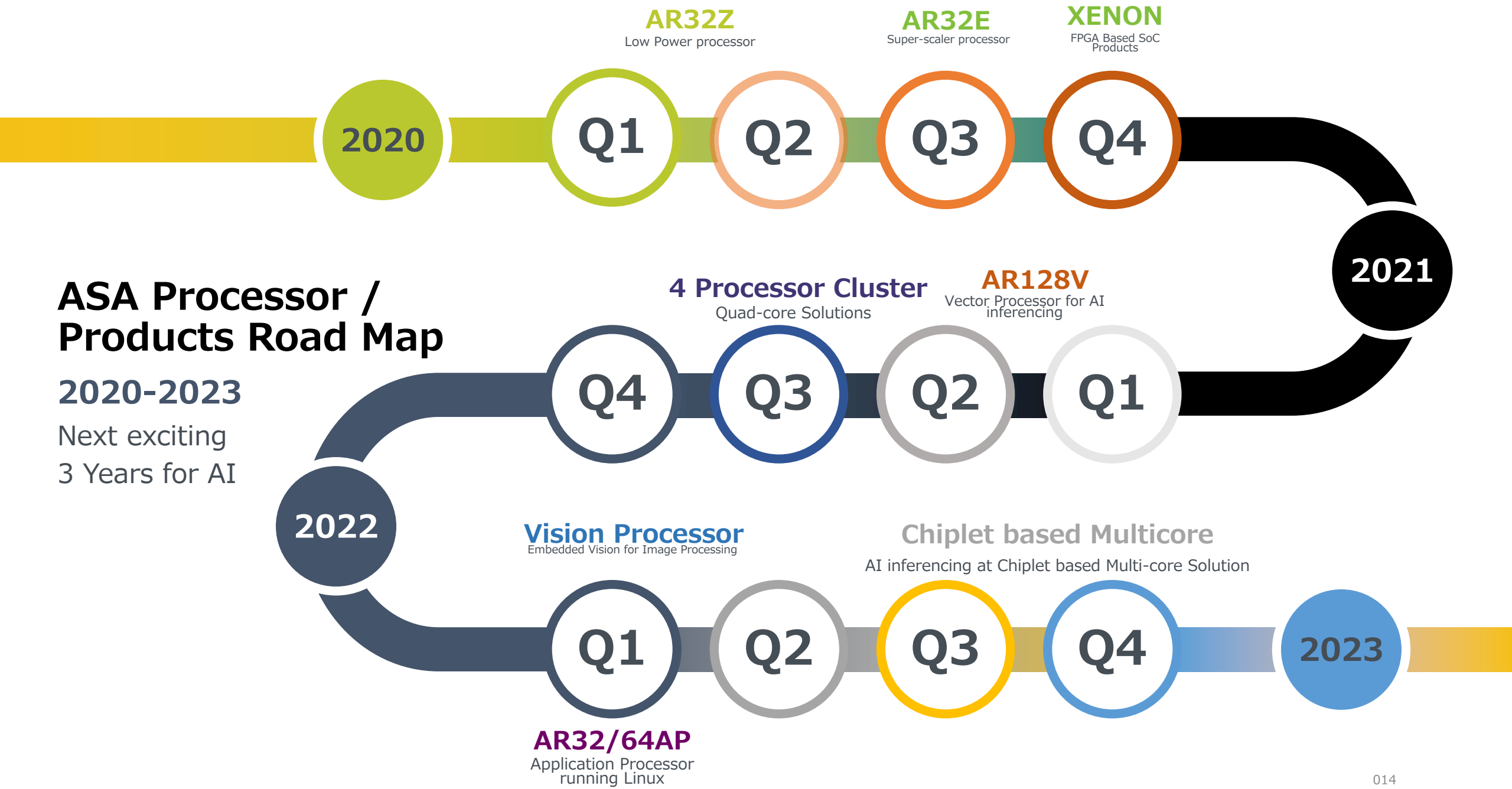
ASA Processor / Products Road Map

2020-2023

Next exciting
3 Years for AI



ASA Edge AI Solutions

- Tightly coupled with ASA Processor
- Low latency
- Low Power
- Complete FPGA solutions available

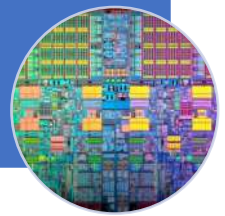
Custom Accelerator

- General Purpose accelerator for all AI/ML applications
- Low Power
- Highly software configurable
- FPGA/ASIC Solution

Vector Processor

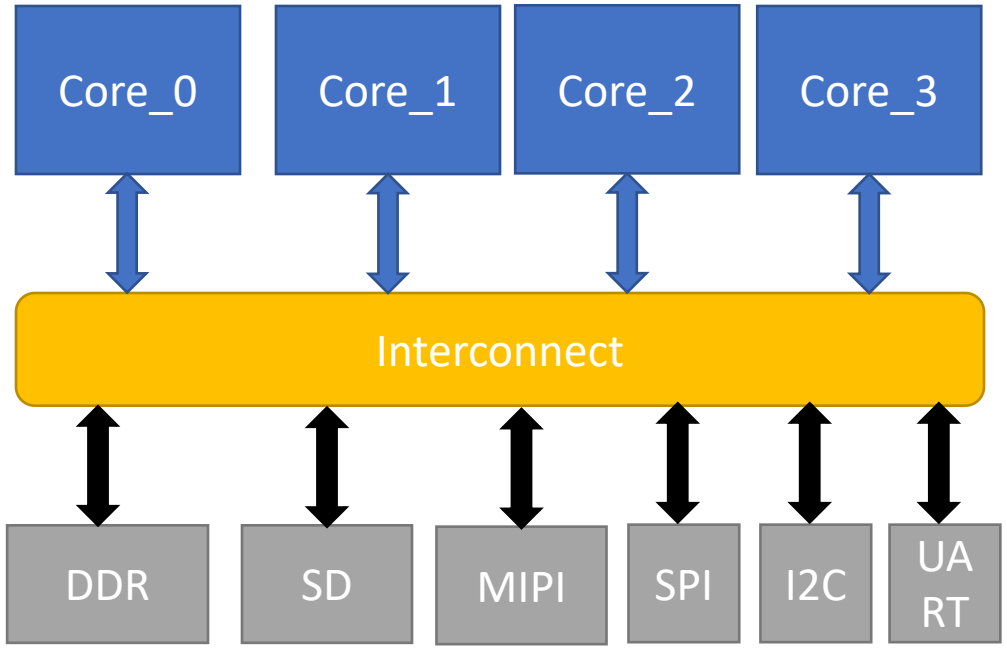
- Heterogeneous low power chiplet based system design
- Highly configurable
- Rapid time-to-market
- Suitable for multiple AI/ML applications including 5G

Multi-Core



ASA RISC-V evaluation board

- FPGA evaluation board, Xenon will enable engineers and students to evaluate and develop their own programs
- It will support FreeRTOS
- Initial release will be single core
- Next releases will contain-
  - multiple processors (up to 4 cores)
  - AI accelerators



ASA Engagement Objectives

- Seeking Strategic Partners to Accelerate ASA Business Success
- Key Elements of Partnership:
  - Product Development:
    - Foundry support
    - Packaging with emphasis on Chiplet technology
    - Accelerator developers
    - Development tools and RTOS

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Thank You