Vision, Mission, and Roadmap of the Jiachen Project

KUBUS Perspective

Weiwei Li, Co-founder and CEO of KUBUDS.
Wei Wu, Co-founder of KUBUDS and Jiachen Project.
2025-02-27

whoami: **Wei Wu @lazyparser**

- **Founder & Manager of the Jiachen Project (2024-)**
- **Co-founder of KUBUDS (2023-)**
- **Founder & Project Director of PLCT Lab, ISCAS(2019-)**

- **TSC Member of**
  - **RVI (rep. ISCAS)**
  - **RISE Foundation (rep. ISCAS)**
- **Board Director of**
  - **CHIPS Alliance (rep. ISCAS)**
  - **LLVM Foundation**

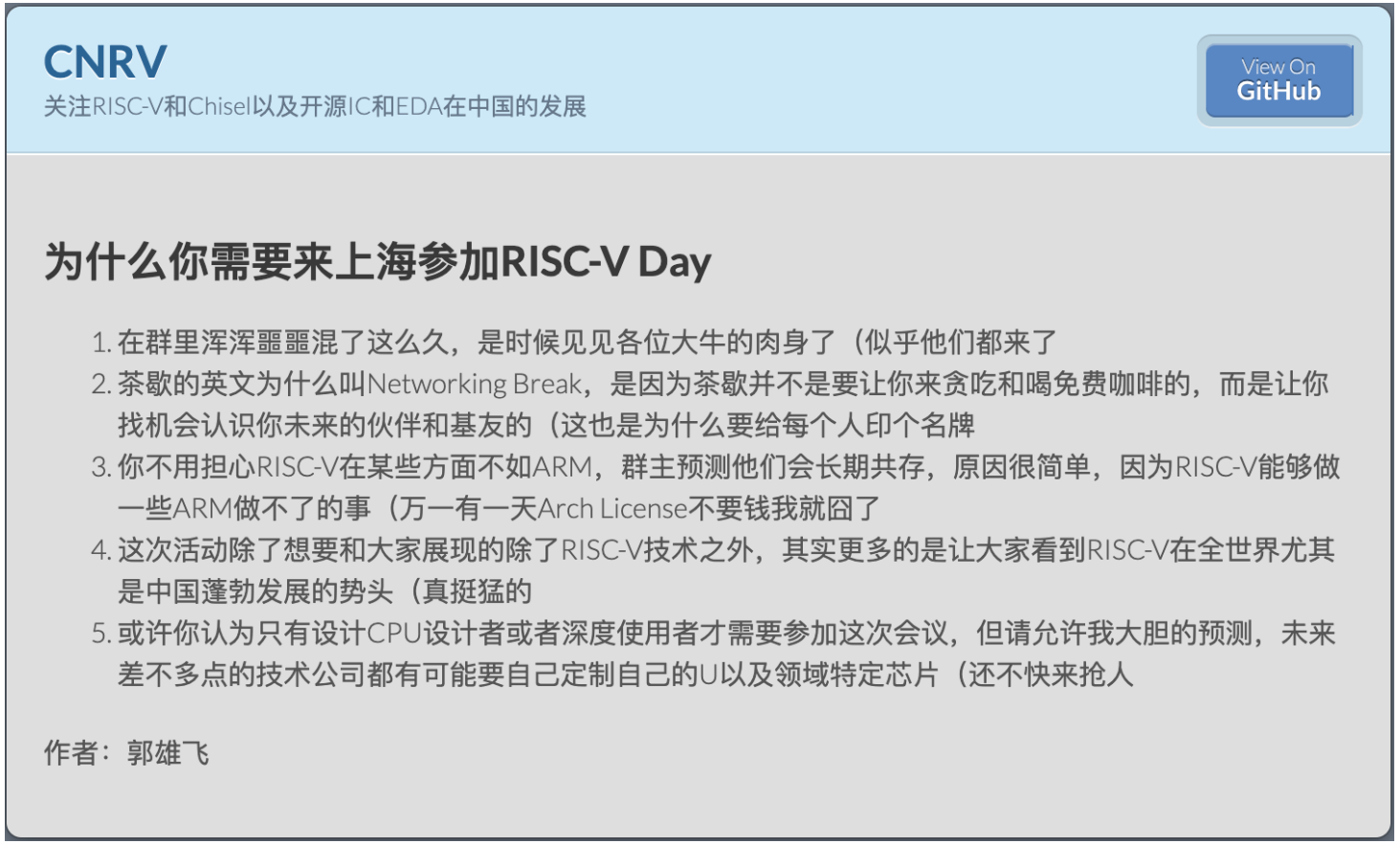
- **RISC-V Ambassador**
- **Core organizer of**
  - **RISC-V Summit China (2021-)**
  - **CNRV (2020-)**
  - **HelloLLVM Community (2018-)**
  - **HelloGCC community (2009-)**

How I met RISC-V and founded the Jiachen Project.

- 2016 - PhD dropout - Serial (unsuccessful) entrepreneurs
  - Dreamed of becoming a compiler engineer & researcher
  - Tried to use ML to improve Firefox JS Engine perf (failed)
  - Worked as a deep learning trainer for a while.
  - Once joined a robotics company (and gradually became CTO)
- Then I met two key people in the future of RISC-V
  - **Alex Guo**,
    - founder of CNRV
      (RISC-V China Community)
  - **Yungang Bao**,
    - founder of the OpenXiangshan
      and One-Student-One-Chip Project

How I met RISC-V and founded the Jiachen Project.

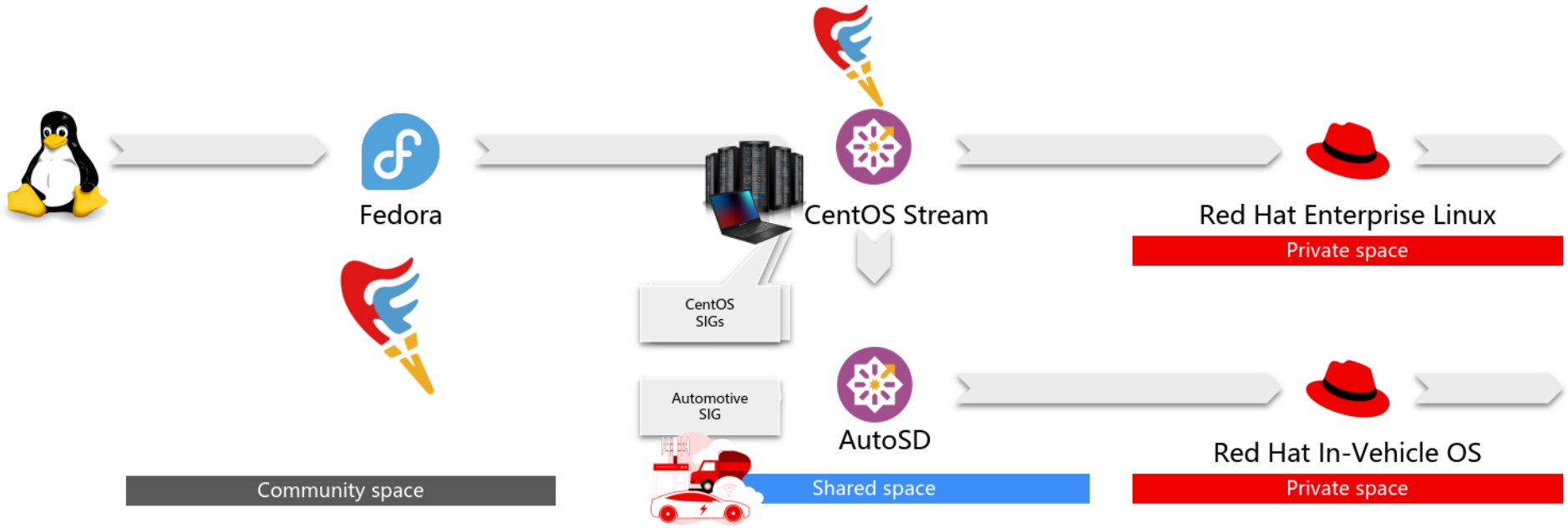
- 2018 - As a sponsor and community builder of RISC-V



Wei Fu
RISC-V Ambassador

RISC-V Ambassador Wei Fu just announced today
(in the adjacent meeting room)

Fedora/CentOS stream/RHEL



We are excited to announce that work is underway on CentOS Stream 10 for the RISC-V architecture within the CentOS ISA SIG.

The Fedora-V Force team is helping to jumpstart the effort.

Red Hat

How I met RISC-V and founded the Jiachen Project.

- 2019 - Returned to ISCAS and founded PLCT Lab
  - The robot startup ran out of money
  - Back to my area of expertise: compilation technology
  - A very ambitious mission and vision has been set for PLCT Lab.
  - Improving the RISC-V backend is a natural entry point into the open source compiler communities.


Mission and Vision of PLCT Lab

The Programming Language and Compilation Technique Lab (PLCT Lab) is committed to

- **becoming an open source leader in the field of compilers,**
- advancing the technological innovation of software **infrastructure** such as **toolchain and runtime system**, and
- possessing the technical and **managerial ability** to lead the development and maintenance of important infrastructure.

At the same time, PLCT Lab is committed to

- **cultivating 10k talents** in the field of compilation and
- promoting the **popularization** and development of advanced compilation technology in China.

How I met RISC-V and founded the Jiachen Project.

- PLCT Lab: Became a development partner and training partner of RISC-V International
  - Probably more than one-third of the FOSS implementations of new RISC-V extension drafts (GCC, LLVM, QEMU, ACT, SAIL, etc.) are implemented and **upstreamed** by engineers or interns from PLCT Lab.

2020 - 2021: Dream big & ambitious

- Porting Google V8 to RISC-V

V8 for RISC-V can now run 'helloworld.js' (only) on RV64GC, with Fedora Developer Rawhide and QEMU

53 views

Wei Wu Jul 15, 2020, 12:45:10 AM

to RISC-V SW Dev, min...@iscas.ac.cn, qi...@iscas.ac.cn

Hi all,

The PLCT lab is excited to announce that we have reached the first milestone of the V8 RISC-V porting project. It can run a single line helloworld.js on RISCV64 platform now.

Although the source code is kinda messy and incomplete, we've decide to open source the ongoing work for discussion. Further, we are aiming to contribute this work to v8 upstream.

The source code could be found at [1] with build instructions [2].

Please drop a issue or reply this mail if you find anything missing or confusing.

[1] https://github.com/isrc-cas/v8-riscv

[2] https://github.com/isrc-cas/v8-riscv/blob/plct-riscv64/README.md

-wuwei

QIU Ji
V8 RISC-V Maintainer
RISC-V Ambassador
Technical Director of PLCT Lab

PLCT Lab and FutureWei team independently implemented V8 RISC-V porting;
Future Wei & RIOS Lab team released the source code ~30 hours later;
and then FutureWei Peng Wu submitted it to upstream as the joint project leader.

2020 - 2021: Dream big & ambitious

- Porting AOSP to RISC-V
  - PLCT only did the preliminary work, and later the XuanTie team, Google, SiFive, etc. did most of the work.

AOSP Porting: The first milestone has been achieved 30 views

Wei Wu (吴伟)
to RISC-V SW Dev
Nov 21, 2020, 4:04:39 PM

Hi all,

The first milestone of Android RISC-V porting has been achieved: now you can boot up the kernel and launch a shell on the QEMU/RV64G.

all the source code (patches) is available at:
https://github.com/aosp-riscv

A detailed article telling how to build and run it is available:
https://zhuanlan.zhihu.com/p/302870095
Unfortunately this blog is written in Chinese. The author, Chen War
https://plctlab.org/

issues and collaborations are always
https://github.com/aosp-riscv/worki

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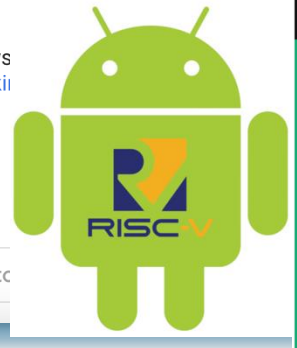
Best wishes,
Wei Wu (吴伟)

Reply all Reply to



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RISC-V Gets an Early, Minimal Android 10 Port Courtesy of PLCT Lab

WANG Chen
Kernel Developer
RT-Thread Guru
MOOC Teacher

2021 - 2022: Dream bigger, then comes TARSIER

We, the PLCT Lab and Tarsier Team[1], are about to start two projects on July 1, 2021:

1. **Porting Firefox to RV64GC, including Spidermonkey w/ JIT support.**

2. **Porting Chromium browser and ChromiumOS to RV64GC.**

The motivation and necessity behind these projects is that we expect there will be **RISC-V laptops** coming out next year. The ISCAS is seeking to build 2000 RV64GC laptops before the end of 2022. I am focusing on the software side...

[Meta Project] Porting Firefox, Chromium/ChromiumOS to RV64GC, Laptop Proect

643 views

Wei Wu (吴伟)
to RISC-V SW Dev

Hi all,

We, the PLCT Lab and Tarsier Team[1], are about to start two projects on July 1, 2021:
1. Porting Firefox to RV64GC, including spidermonkey w/ JIT support.
2. Porting Chromium browser and ChromiumOS to RV64GC.

All the roadmaps, development meetings, CI/BuildFarm, source codes and issue trackers will be open in July. All the codes will be submitted to upstreams eventually.

The motivation and necessity behind these pro
there will be RISC-V laptops coming out next ye
seeking to build 2000 RV64GC laptops before t
focusing on the software side. There are still a
the RISC-V software ecosystem which should b
hardwares is ready. The availability of mainstre
currently the highest demand we heard.

Collaborations are welcome! Feel free to name
RISC-V software ecosystem so that we can do
priority.

[1] Tarsier Team is a new team in ISCAS, which
and optimizing Linux distributions for RISC-V.

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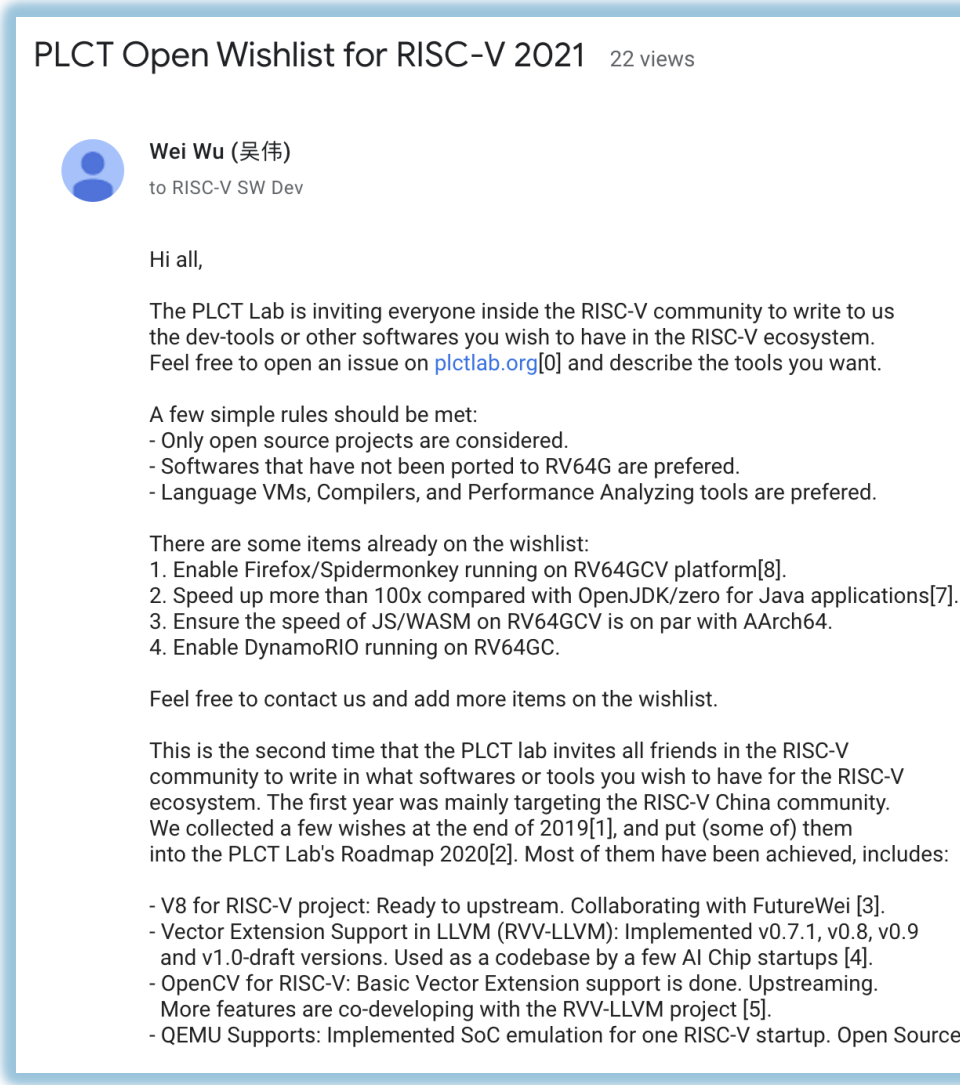
Best wishes,
Wei Wu (吴伟)

Junqiang Wang
Head of
TARSIER Team

2021 - 2022: Dream bigger, then comes TARSIER

Some items already on the Wishlist:

1. Enable **Firefox/Spidermonkey** running on RV64GCV platform[8].
2. Speed up more than **100x** compared with **OpenJDK**/zero for Java applications[7].
3. Ensure the **speed of JS/WASM** on RV64GCV is on par with AArch64.
4. Enable **DynamoRIO** running on RV64GC.



PLCT Open Wishlist for RISC-V 2021 22 views

Wei Wu (吴伟)
to RISC-V SW Dev

Hi all,

The PLCT Lab is inviting everyone inside the RISC-V community to write to us the dev-tools or other softwares you wish to have in the RISC-V ecosystem. Feel free to open an issue on plctlab.org[0] and describe the tools you want.

A few simple rules should be met:
- Only open source projects are considered.
- Softwares that have not been ported to RV64G are prefered.
- Language VMs, Compilers, and Performance Analyzing tools are prefered.

There are some items already on the wishlist:
1. Enable Firefox/Spidermonkey running on RV64GCV platform[8].
2. Speed up more than 100x compared with OpenJDK/zero for Java applications[7].
3. Ensure the speed of JS/WASM on RV64GCV is on par with AArch64.
4. Enable DynamoRIO running on RV64GC.

Feel free to contact us and add more items on the wishlist.

This is the second time that the PLCT lab invites all friends in the RISC-V community to write in what softwares or tools you wish to have for the RISC-V ecosystem. The first year was mainly targeting the RISC-V China community. We collected a few wishes at the end of 2019[1], and put (some of) them into the PLCT Lab's Roadmap 2020[2]. Most of them have been achieved, includes:

- V8 for RISC-V project: Ready to upstream. Collaborating with FutureWei [3].
- Vector Extension Support in LLVM (RVV-LLVM): Implemented v0.7.1, v0.8, v0.9 and v1.0-draft versions. Used as a codebase by a few AI Chip startups [4].
- OpenCV for RISC-V: Basic Vector Extension support is done. Upstreaming. More features are co-developing with the RVV-LLVM project [5].
- QEMU Supports: Implemented SoC emulation for one RISC-V startup. Open Source

2021 - 2022: Dream bigger, then comes TARSIER

- The goal of the **TARSIER Project** is to promote **support for the RISC-V platform in mainstream Linux distributions** (including Debian/Ubuntu, Fedora, Arch Linux, Gentoo, openEuler, etc.) to match or exceed the level of support for the AArch64 platform.
- **Make RISC-V the Tier-1 architecture for all open-source projects.**
- **Port all popular Linux distributions to RISC-V Laptops with OA suites.**
- **Complete the porting of HPC computing software packages.**

https://commons.wikimedia.org/wiki/File:Libre_office.png.png

https://commons.wikimedia.org/wiki/File:LuaJIT_Orange_on_Blue_Logo.png

https://en.m.wikipedia.org/wiki/File:Node.js_logo.svg

2021 - 2022: Dream bigger, then comes TARSIER

RISC-V is the future. We're seeing it.

In 2022, (almost) all the popular Linux distros support RISC-V. Linux Desktop is almost there.

TARSIER

Distros	Ubuntu	openKylin	Deepin	**openEuler**	OpenCloudOS	OpenWRT	OpenBSD	RT-Thread	Yocto
	Debian	Fedora	Gentoo	Arch Linux	FreeBSD	openAnolis	ChromiumOS	FreeRTOS	Buildroot

Lang & Runtime	C/C++/Fortran/Rust GNU GCC, Clang/LLVM	Java OpenJDK	JavaScript V8, NodeJS, Spidermonkey	Go / WASM Upstreamed	Dart Upstreamed	C# / .NET N/A

PLCT Lab

If you find any open source software that you would like to run on RISC-V but are not yet supported, **feel free to email me**. I will be looking for financial resources and volunteers to get it done.
My address is “Wei Wu <wuwei2016@iscas.ac.cn>”

- Very Good Support
- Good Support
- Basic Support
- N/A

2023: TARSIER ends, followed by KUBUDS

- PLCT & TARSIER Team ran out of funds
  - TARSIER Project terminated; members disbanded
  - PLCT Lab laid off 50% of its staff; Simulator team disbanded
- In the fall of 2023, a few core partners from PLCT and TARSIER teams joined together to form KUBUDS Co., Ltd., dedicated to inheriting and continuing TARSIER's mission and vision.

苦芽KUBUDS

Shanghai KUBUDS Technology Co., Ltd.

- More than 10 years of experience in fundamental software such as compilers, virtual machines and simulators.
- Deep participation in RISC-V ecosystem.
- Committed to providing solid commercial support for enterprises and teams engaged in chip designing and innovation.
- https://kubuds.io/

Weiwei Li
CEO, KUBUDS
ex-head of
PLCT Simulators

Junwiang Wang
CTO, KUBUDS
ex-head of
TARSIER

苦芽 KUBUDS

2023: TARSIER ends, followed by KUBUDS

RISC-V is the future. We're seeing it.

In 2022, (almost) all the popular Linux distros support RISC-V. Linux Desktop is almost there.

KUBUDS provides commercial RISC-V services covering all popular Linux distributions

Distros	Ubuntu	openKylin	Deepin	**openEuler**	OpenCloudOS	OpenWRT	OpenBSD	RT-Thread	Yocto
	Debian	Fedora	Gentoo	Arch Linux	FreeBSD	openAnolis	ChromiumOS	FreeRTOS	Buildroot

Lang & Runtime	C/C++/Fortran/Rust GNU GCC, Clang/LLVM	Java OpenJDK	JavaScript V8, NodeJS, Spidermonkey	Go / WASM Upstreamed	Dart Upstreamed	C# / .NET N/A

KUBUDS provides commercial RISC-V services covering all important Simulators and Compilers

If you find any open source software that you would like to run on RISC-V but are not yet supported, **feel free to email me**. I will be looking for financial resources and volunteers to get it done.
My address is “Wei Wu <wuwei2016@iscas.ac.cn>”

Very Good Support
Good Support
Basic Support
N/A

2024: We need to dream bigger, much bigger

- RISC-V has become the de facto standard in the ISA field.
  - Look around!
- There is no need to worry about the huge momentum of the global open source software ecosystem supporting RISC-V.
  - **PLCT & KUBUDS can provide good support.**
- However, the global **commercial software** still has a wait-and-see attitude towards RISC-V. Although they actively support it verbally, most companies do not have a timetable for investment and delivery.
  - **This is why I started the Jiachen project.**

Jiachen Project (甲辰计划):

An ambitious plan spanning 12 years

2024 (Jiachen) -> 2036 (Bingchen)

Why another project?

The RISC-V Commercial prosperity

requires someone to solve the problem of

First-mover disadvantage

Jiachen Vision

- RISC-V is the future of computing.
- All IT areas involving ISA will be covered by RISC-V.
- Open standards and open source software and hardware ecosystem will become the cornerstone of business prosperity.
- With our joint efforts, RISC-V will achieve commercial prosperity in all fields within 12 years.

Mission & Goals

- Bringing a joint effort of over 100 chip and solution makers and over 500 ISVs, to port, optimize, and **deploy over 1,000 key commercial software across all fields.**

Mission & Goals

- Bringing a joint effort of over 100 chip and solutions manufacturers and over 500 ISVs, to port, optimize, and deploy over 1,000 key commercial software across all fields.

- Developing **solutions** suitable for commercial applications around high-performance RISC-V chips and IPs such as SG2380 and XiangShan, helping our target industries. These industries include **AI acceleration, edge computing, storage, robotics, simulation, computer-assisted medical solutions**, and more.

Mission & Goals

- Bringing a joint effort of over 100 chip and solutions manufacturers and over 500 ISVs, to port, optimize, and deploy over 1,000 key commercial software across all fields.
- Developing solutions suitable for commercial applications around high-performance RISC-V chips and IPs such as SG2380 and XiangShan, helping our target industries. These industries include AI acceleration, edge computing, storage, robotics, simulation, computer-assisted medical solutions, and many more.
- Building a human resource development effort for RISC-V **to network over 10k potential experts in RISC-V** chip design, software development, community management, as well as education and training. This will allow us to enable an industry-wide human resource network.

The goals are based on **three fundamental observations**

- **Moore‘s Law is dead, and the demand for computing power is surging.**
- **The complexity of software is growing superlinearly, exceeding the management limit of any organization.**
- **Engineers who can manage software complexity are scarce worldwide. And we have not yet found a way to cultivate them.**

The goals are based on **three fundamental observations**

- **Moore‘s Law is dead, and the demand for computing power is surging.**
  - **DSA has become a key path to improving performance.**
- **The complexity of software is growing superlinearly, exceeding the management limit of any organization.**
  - **The global open source software ecosystem has become the foundation of all commercial software.**
- **Engineers who can manage software complexity are scarce worldwide. And we have not yet found a way to cultivate them.**
  - Only by relying on the top open source software can we survive and develop.
  - Only one or two open source software survive and prosper in each niche.
  - **DSA will also be open source, and only one will survive.**
  - **Then winner is RISC-V.**

How is Jiachen Project organized?

- **Manifesto style: Any company or developer that shares the vision is welcome to join and free to quit.**
- **All members are equal.**
- **Members can unite freely to accomplish a specific goal. Founding members need to raise funds themselves.**
- **The more you contribute, the greater your impact.**

https://github.com/rv2036/jiachen-community

No Governance, No Financial Model

- **No financial entity.**
  No membership fees.
  No donations.
- **No board.**
  Only one manager Wei Wu,
  who is responsible for contacting and sharing information among members.
- **No (regular) meetings (yet).**

The Portfolio needs no money:

- **Website: https://rv2036.org**
- **GitHub: gh/rv2036**
- **WeChat account.**
- **X (Twitter) account.**
- **WeChat video account.**
- **YouTube account.**

The first driving force of the Jiachen Project

- Members don’t pay for what they don’t want.
- Members can create new projects according to their own needs and share the ideas among all members directly.
- The manager (Wei Wu) collects and summarize member needs and form a list of open projects for analysis and sponsorship by interested groups.
- As the starting momentum of Jiachen project, **PLCT Lab and KUBUDS** provide engineers and interns to help improving the open source software ecosystem for the RISC-V community.

PLCT Lab & KUBUDS: Very powerful push

- Infra, CI/CD
  - **RISC-V board farm hosting**
  - RISC-V Ecosystem Lab
- Developer tools
  - DynamoRIO
  - RuyiSDK
  - **QEMU & Spike**
  - **Gem5 & Sparta**
- C/C++/Fortran toolchain support
  - GNU Toolchain
  - **Clang/LLVM**
  - Go
- Language runtime support
  - JS Engines: V8, Spidermonkey.
  - Java VM: OpenJDK/Hotspot
  - Lua: LuaJIT
  - Others: Box64, **Wine-CE**
- **OS Porting and system optimization**
  - **KarsierOS, Arch Linux, Gentoo, Deepin, Debian/Ubuntu, etc.**
  - **RT-Thread / Smart**
- AI Stack
  - **MLIR**
  - Buddy Compiler / T1

Three common funding models

- **Single Dominant Player**
  A niche is dominated by one company.
  Vertically integrated enterprise, from IP-SoC-Board-Product to Sales

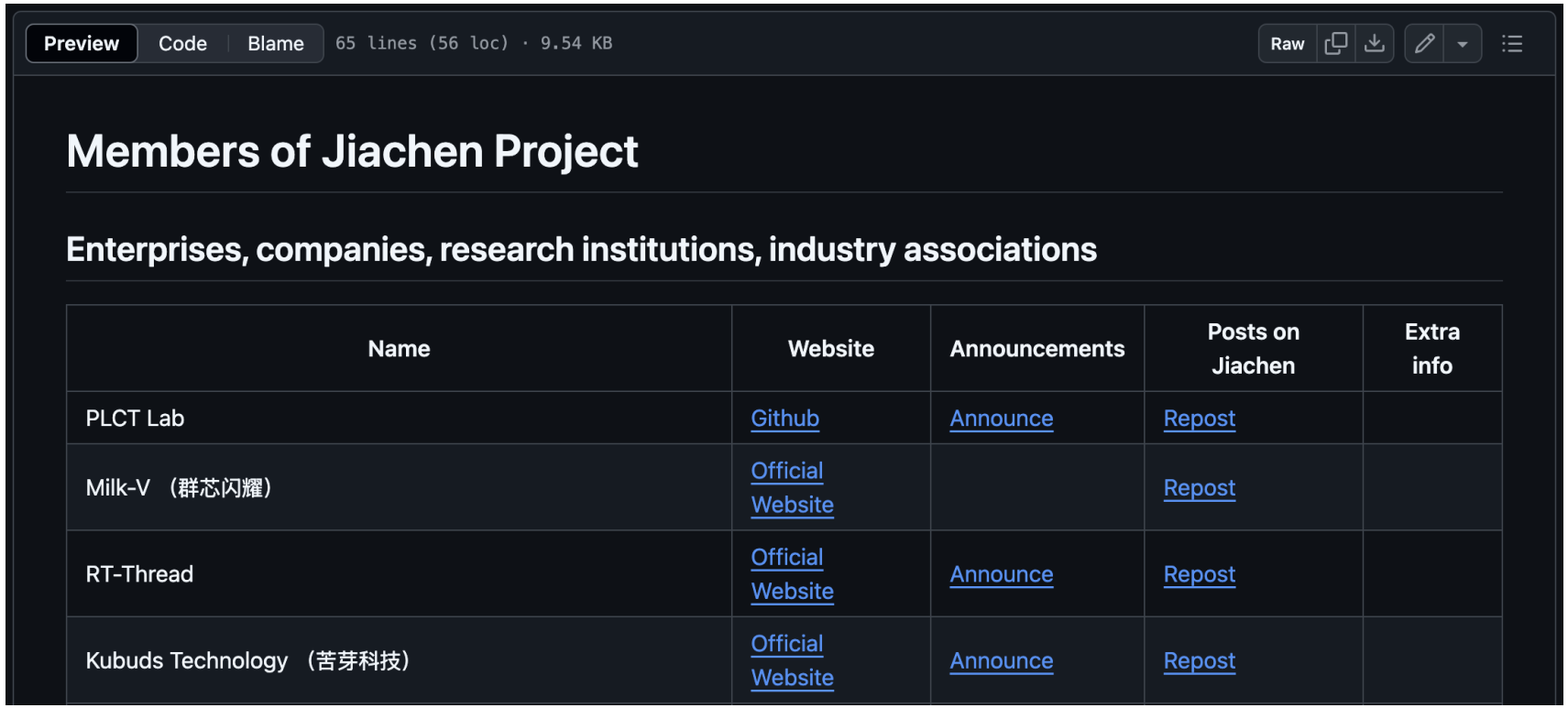
- **Combine the majority of players**
  The market share of a segment is mainly covered by the products or services of 3-7 companies.

- **National or Gov support**
  Very dispersive, or strong externalities. (e.g. PLCT Lab & TARSIER)

Wait! So, what we are talking about is an organization without any funds, relying on only one person's voluntary coordination, hoping to directly decide the use of 1 billion RMB and indirectly promote a market value of 100 billion RMB.

Is this really possible?

More than 40 RISC-V companies have joined the Jiachen Project, including 3 of the top 4 global RISC-V IP companies*



Preview | Code | Blame | 65 lines (56 loc) · 9.54 KB | Raw

Members of Jiachen Project

Enterprises, companies, research institutions, industry associations

Name	Website	Announcements	Posts on Jiachen	Extra info
PLCT Lab	Github	Announce	Repost	
Milk-V （群芯闪耀）	Official Website		Repost	
RT-Thread	Official Website	Announce	Repost	
Kubuds Technology （苦芽科技）	Official Website	Announce	Repost	

https://github.com/**rv2036**/jiachen-community/blob/main/members.md

(* based on 2023 SHD Group data)

≥40 companies, communities, and research groups joined*
≥100 individual developers joined

RuyiSDK
all-in-one Toolbox

PLCT

XuanTie玄铁

milkV

算能 SOPHGO

SiPEED 矽速科技

SPACEMIT 进迭时空

New ILP32 Solution
RV64ILP32

XuanTie玄铁

嘉楠 canaan

PLCT

RT-Thread

RVSPOC

苦芽

算能 SOPHGO

XuanTie玄铁

FOSS Internship
Joint Recruitment
and Training

PLCT milkV

PerfXLab 澎峰科技

苦芽

inchi 英麒智能

WCH 沁恒

RT-Thread

Vulab Tech 中科微澜

riscvpedia
For non-developers

苦芽

PLCT

These are only part of Jiachen Project. More interesting projects in the slides that follow!

RISC-V Dev Boards Wandering Project

Every RISC-V development board deserves to be plugged in and loved!

https://github.com/rv2036/riscv-board-wandering

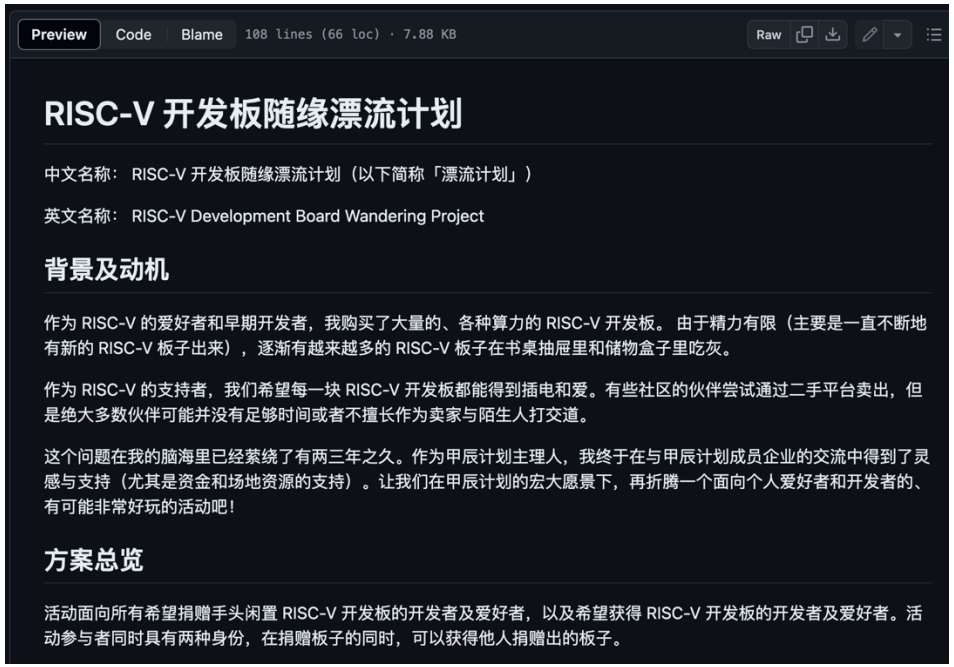
RISC-V Dev Boards Wandering Project

- Very interesting project. RISC-V dev boards can be donated and earn wandering points. Boards donated by vendors can be counted as wandering points.
- Users with wandering points ≥0 can request a development board. All donations and acquisitions are optimistically opportunistic and not mandatory.
- Sort of honorary list of RISC-V contributions.
- A new system built from scratch with almost no additional costs introduced. Vendors are happy, experienced enthusiasts are happy, and newcomers are happy.

The wandering system is up and running

≥10 vendors and individuals donated.

≥80 developers got boards.



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RISC-V 开发板随缘漂流计划

中文名称： RISC-V 开发板随缘漂流计划（以下简称「漂流计划」）

英文名称： RISC-V Development Board Wandering Project

背景及动机

作为 RISC-V 的爱好者和早期开发者，我购买了大量的、各种算力的 RISC-V 开发板。由于精力有限（主要是一直不断地有新的 RISC-V 板子出来），逐渐有越来越多的 RISC-V 板子在书桌抽屉里和储物盒子里吃灰。

作为 RISC-V 的支持者，我们希望每一块 RISC-V 开发板都能得到插电和爱。有些社区的伙伴尝试通过二手平台卖出，但是绝大多数伙伴可能并没有足够时间或者不擅长作为卖家与陌生人打交道。

这个问题在我的脑海里已经萦绕了有两三年之久。作为甲辰计划主理人，我终于在与甲辰计划成员企业的交流中得到了灵感与支持（尤其是资金和场地资源的支持）。让我们在甲辰计划的宏大愿景下，再折腾一个面向个人爱好者和开发者的、有可能非常好玩的活动吧！

方案总览

活动面向所有希望捐赠手头闲置 RISC-V 开发板的开发者及爱好者，以及希望获得 RISC-V 开发板的开发者及爱好者。活动参与者同时具有两种身份，在捐赠板子的同时，可以获得他人捐赠出的板子。

- **Fully open, highly transparent, and**
- **possibly unprecedented way to connect (in the future) tens of thousands of developers and hundreds of vendors**
  - **in a loosely coupled way to contribute to the RISC-V ecosystem together.**

Thank you, donators and dockbase managers!

English Name	Wandering Points	Extra Info
sophgo	2640	开发板赞助厂商
sipeed	27550	开发板赞助厂商
milk-v	10660	开发板赞助厂商
SpacemiT	2498	开发板赞助厂商
SiFive	24500	开发板赞助厂商
RISC-V International	3596	RVI DevBoards Program
qinware	2916	生产力工具软件提供商
XuanTie	267880	xrvm.cn

This page lists the wandering points earned by companies that donated RISC-V development boards.
Data collection time is January 1, 2025

Thank you, donators and dockbase managers!

Dockbase Name	Points	Manager	Organizer
南京漂流基地	120	陈曦	英麒智能
深圳漂流基地	0	柯一冉	群芯闪耀
上海漂流基地	0	王文君	苦芽科技
杭州漂流基地	180	王文君	苦芽科技
广州漂流基地	0	吴伟(临时兼任)	广州市智能软件产业研究院（PLCT实验室南沙分部）
北京漂流基地	0	安旭	北京开源芯片研究院（BOSC）
合肥漂流基地	0	TBD	合肥工业大学数学学院
大连漂流基地	0	TBD	大连理工大学

This page lists wandering dockbases in various cities where member companies of the Jiacheng Project offer volunteering services.

甲辰计划主理人发起开源实习生联合招聘培养项目

Original 甲辰计划主理人 甲辰计划 2024-06-09 02:57 浙江

News on Jiachen Project Launched Joint Recruitment and Development of RISC-V FOSS Internships

项目名称

甲辰计划开源实习生联合招聘培养

项目目标

自甲辰龙年开始，甲辰计划成员单位授权甲辰计划主理人招募实习生从事开源RISC-V相关工作，**每年开放总额超过2000名实习名额。**甲辰计划主理人招募至少1000名高校学生参与实习。

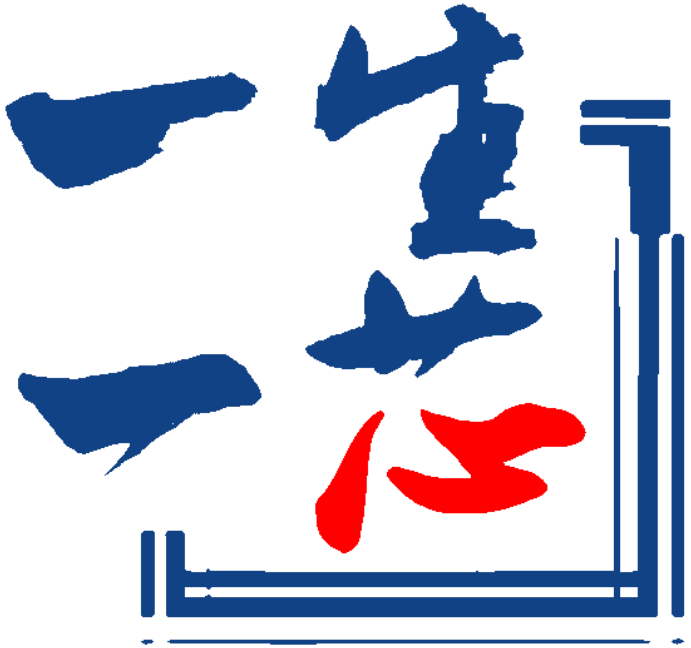
经费形式

Joint Internship Recruitment is up and running

- ≥2,300 hc promised
- ≥350 interns onboarded
- ≥10 companies
- ≥50 mentors
- ≥40 FOSS projects
  - GCC, LLVM, QEMU, Linux
  - openEuler, Fedora, Debian
  - V8, box64, OpenCV, etc.

Joint Internship Recruitment is up and running

- https://github.com/rv2036/weloveinterns/blob/master/open-internships.md



The Jiachen Project announced the recognition of the new CBAS certification system for the “One Student One Chip” program. Certified students will automatically receive internship offers from the FOSS internship joint training program of Jiachen Project.

日本語翻訳ボランティアチーム募集中！
The default is Simplified Chinese. English translation will be released gradually. Japanese translation has not started yet, and the volunteer team is actively recruiting!

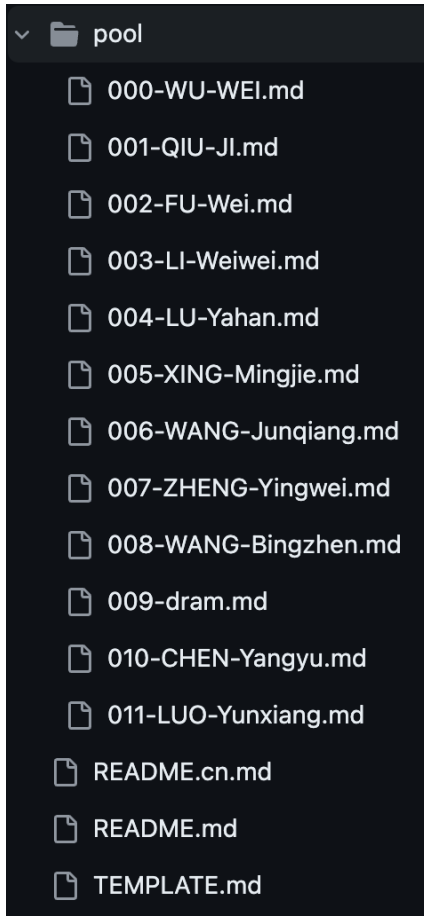
RISC-V talent identification and mutual recognition

It all started with endorsement number 0

- Pure person-to-person endorsement
- Wei endorsed himself as No.0000
- Endorsement issued by Wei Wu for talents starting from NO.0001
- All endorsements are public online

https://github.com/rv2036/**jiachen-builders-network**

RISC-V Talent Recognition Network has issued ≥17 endorsements



邱吉 (QIU Ji)

NO: 001

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- LinkedIn: TBA (Optional)
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- WeChat: (No need to publish by default)
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Brief Bio

邱吉，中科院软件所PLCT实验室技术总监。2007年本科毕业于南开大学计算机科学与技术系，2013年博士毕业于中科院计算技术研究所微处理器研究中心龙芯团队，研究方向为微处理器软硬件协同设计和优化。在工具链、虚拟机等技术领域有10年以上经验。其任职的PLCT实验室，面向编译器、虚拟机、模拟器技术，专注于在这些领域推动RISC-V指令集架构支持，已经成为RISC-V国际基金会和OpenHW Group的活跃贡献者。在加入PLCT实验室之前，担任过展讯通信自研CPU、XPU部门编译器和基础库负责人、龙芯团队芯片部基础软件组负责人等职务。她长期致力于开源软件社区推广和贡献，担任HelloLLVM社区负责人。在2023年，发起和推出了「南盘江计划」，致力于帮助更多的女性工程师在编译等基础软件领域实现个人职业目标。

Capabilities (aka. The scope of the issuer's endorsement)

- 作为管理者和运营者，有能力从零开始组建起一个高效能的技术团队，在高压力环境下完成交付。
- 作为技术专家，在微处理器软硬件协同设计优化领域有着丰富的经验。
- 作为技术专家，在LLVM工具链领域有着扎实的理论和工程实践经验，带领PLCT实验室交付过多个商业项目。
- 作为技术专家，在V8等语言虚拟机领域有着丰富的研发和维护经验，是 V8 RISC-V 后端 Maintainer。
- 作为管理者，具备开源社区运营和培育能力。
- 作为调停人，极强的团队协调和多组织混合场景协调能力。
- 作为教育者，培养了近百名开源实习生和编译器工程师；具备初步的危机干预能力。

Issuer

甲辰计划主理人吴伟（000 WU Wei）

Recommendation from the issuer

我在此为邱吉博士背书，邱吉博士在PLCT实验室担任技术总监期间，展示了上述所有能力。

I hereby endorse Dr. Qiu Ji, who demonstrated all of the above abilities during his tenure as Technical Director at PLCT Laboratory.

Issuer Guarantee Period

Time of issuance: 2024-06-29

Validity period of issuance (default 5 years): 2036-12-31

郑英炜 (ZHENG Yingwei)

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Brief Bio

郑英炜，2024年本科毕业于南方科技大学，现为南方科技大学硕士研究生。2023年加入PLCT实验室实习，作为 LLVM committer 从事 LLVM 编译系统优化器、RISC-V 后端的开发与 Code Revew 工作。近一年提交并合入主线的补丁共239个， monorepo 排名前30；积极参与社区事务，处理了上百个来自学术界和下游用户的issue，被邀请审核了上百个PR，并参与了一部分设计讨论；依托多维度持续性能监测系统，多次在补丁合入前发现优化错误/性能劣化，提升了LLVM的可靠程度以及编译产物在RISC-V平台上的性能；推进多个RISC-V扩展在LLVM编译工具链的落地，并将国产第二代香山处理器南湖高性能核的微架构支持合入主线；指导十多个新人（部分为国内开发者）参与LLVM开发，有部分开发者已成为committer并持续活跃于LLVM社区。向Alive2翻译验证工具贡献多个 issues/PRs，保障了LLVM的优化正确性以及 LLVM IR 改进实验的进行。

Capabilities (aka. The scope of the issuer's endorsement)

- 在编译器优化、测试与验证方面积累了丰富的理论知识与实践经验。具备独立构建 CI 基础设施并持续进行观测的能力，有丰富的快速定位缺陷根因并修复的经验。
- 具备宽泛的技术视野，了解不同领域应用的代码模式与性能瓶颈，并在编译优化相关讨论中提供来自真实应用场景的例子。
- 工程能力强，能基于已有工作快速搭建出原型并验证。
- 有着出色的社区沟通和运营能力，并且能够根据公开信息综合汇总得到未被发现过的趋势判断，并与多个国内外顶级研究团队（软件工程、安全、体系结构等方向）建立了个人连接并提供过技术支持。

Issuer

甲辰计划主理人吴伟（000 WU Wei）

Recommendation from the issuer

我在此为郑英炜同学背书。郑英炜同学在实习期间体现了超过 LV4 的能力，能够在 LLVM 等编译器技术领域独立的展开一个新的基础设施和流程体系，并且能够围绕自己搭建的体系，建立起与实习生和全职员工对接协作的体系流程。

Issuer Guarantee Period

Time of issuance: 2024-07-05

Validity period of issuance (default 5 years): 2027-12-31

RISC-V User Documentation Encyclopedia Project

riscvpedia.org

- Part of the Jiachen Project
- For the First 50M RISC-V Users
- Launched at the RISC-V China Summit on August 23 st, 2024.
- KUBUDS initiated the program and acted as the lead organization.
- ≥7 vendors joined, including Milk-V, Sipeed, PLCT Lab, etc.

Projects that are still in the pipeline but not yet on track (planned to be completed in 2025)

- RVPOC: RISC-V Software Porting & Optimization Challenge
- RISC-V Chip Security Challenge
  - The OpenXiangshan RTL/chip as the main targets
- Offensive paper reading group
  - RISAT tool project
- RISC-V Document Encyclopedia
- Multi-language Translation Team
- Industry Case Demonstration
- Contribution Nomination Committee

The most important elements leading to the RISC-V ecosystem and commercial prosperity are: developers.

It’s all about developers

From novice to expert, from user to contributor,
from applicant to donor, from learner to mentor.

Welcome to join the Jiachen Project

https://rv2036.org

https://github.com/rv2036

lazyparser@gmail.com